A New Interpolation Technique for TI $\Sigma\Delta$ A/D Converters

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Abstract—Time interleaved sigma-delta converter is a potential candidate for multi-mode wideband analog to digital (A/D) converters dedicated for multistandard receivers. However, the interpolation by zeros required to compress the useful signal bandwidth at the input of the sigma-delta modulator imposes constraints on the implementation of the analog part leading to a very large die area due to the high value required for the sampling capacitor. This paper proposes a new interpolation technique using extra samples instead of zeros resulting from the oversampling of the input signal. This new technique not only reduces the die area but also the anti-alias filter order. The proposed technique was validated in a 4 channel time interleaved sigma-delta multi-mode A/D converter designed in 1.2 V 65 nm CMOS process.

Index Terms—sigma-delta, analog-to-digital conversion, interpolation, time-interleaving.

INTRODUCTION

The current evolution of telecommunication systems moves toward versatile, reconfigurable and multistandard receiver. In this context, the concept of software radio [1] and cognitive radio presents an interesting solution to reach these requirements allowing optimal management of the frequency resources in the radio environment and introducing the dynamic reconfiguration for multistandard applications. In the radio frequency front-end of the receiver, the main idea consists on moving the A/D converter as near as possible to the antenna. The A/D converter suitable for this application must be capable of a bandwidth-resolution exchange to ensure multistandard reception while maintaining low power consumption.

Widening the conversion bandwidth of the A/D converters while ensuring high resolution remains a bottleneck to overcome. Sigma-delta ($\Sigma\Delta$) converters are good candidates to achieve high resolution conversion but their bandwidth is very narrow compared to the requirements needed for software radio applications. Several parallelism techniques allow to increase $\Sigma\Delta$ conversion bandwidth: Time Interleaved sigma-delta (TII$\Sigma\Delta$) [2], Parallel sigma-delta (PI$\Sigma\Delta$) [3], and Frequency Band Decomposition (FBD) [4]. The TII$\Sigma\Delta$ solution has the lowest hardware complexity among the three possible techniques and offers the easiest way for reconfiguration. It uses the same $\Sigma\Delta$ modulator for all channels and requires reasonable digital resources [5].

The main challenge in the implementation of this architecture lies in securing a high resolution. In fact, the interpolation required to compress the useful signal bandwidth at the input of the sigma-delta modulator is carried out by inserting zeros between every two adjacent samples of the input signal sampled at the Nyquist rate. As a consequence, the useful signal power is decreased and therefore to maintain the same signal power to thermal noise power ratio, high value for sampling capacitor is needed.

To overcome this problem, this paper presents a new interpolation technique based on oversampling. This technique was validated in a 4 channel TII$\Sigma\Delta$ reconfigurable A/D converter suited for GSM, UMTS, EDGE, WiFi and WiMax. It was designed in a 1.2 V 65 nm CMOS process.

The first section of this paper describes the principle of TII$\Sigma\Delta$ A/D converters. It presents also the implementation constraints of the analog components of the TII$\Sigma\Delta$ A/D converter. Section II sheds light on the new interpolation technique for reducing implementation constraints. In section III, the implementation of the new interpolation technique is presented and the performance of this technique is evaluated using the 4 channel TII$\Sigma\Delta$ A/D converter prototype presented in section IV.

I. CLASSICAL TIME INTERLEAVED SIGMA-DELTA ARCHITECTURE

A. Principle

The simplified schematic of a TII$\Sigma\Delta$ A/D converter is depicted in Fig. 1. The architecture is composed of $M$ parallel low-pass $\Sigma\Delta$ modulators. The analog input signal is sampled at the Nyquist rate $f_s$. Then, the signal $x[n]$ is distributed among the $M$ modulators through an analog multiplexer and interpolated by a factor $N$ to compress the useful signal bandwidth. The signal then goes through the $\Sigma\Delta$ modulator and the quantization noise shaping is carried out. Afterwards, the output of each modulator is filtered by the digital filter $H(z)$ to suppress the out of band quantization noise. Finally, the signal is decimated by a factor $N$ to reduce the data rate before being demultiplexed by a digital demultiplexer to reconstruct the output signal $y[n]$.

B. Analog implementation

Fig. 2 shows one way to implement the frond-end of a TII$\Sigma\Delta$ A/D converter using switched capacitor (SC) technology. For the sake of simplicity, a single-ended representation is illustrated. In Fig. 2, the S/H and 1st channel analog multiplexer and 1st integrator are illustrated. The S/H was placed before all channels to avoid clock skew. Other techniques such as global passive sampling [7] and clock calibration [8] can be used instead but they may not be as efficient as the S/H approach.

As shown in Fig. 2, an analog multiplexer is placed between the S/H and the 1st integrator of all channels. It consists of just 2 switches: the first one processes signal samples and the other one is connected to the common mode to acquire zero values. The clock signals that control the multiplexer are generated in the interpolation network that will be discussed later in section III. This network generates clock signals that perform the decimation by $M$ and the...
interpolation by \( N \), just before the modulator as shown in Fig. 1. The other clock signals are represented in Fig. 2. The delayed versions of the clocks decrease the charge injection and make it signal independent.

One of the advantages of the \( \text{TI} \Delta \Sigma \) A/D converter is the capacity to perform a Nyquist conversion. However, in high resolution applications, it requires very high value of sampling capacitors because the thermal noise must be lower than the quantization noise defined by the converter resolution. Therefore, the sampling capacitor \( C_{sS/H} \) of the \( S/H \) and \( C_{sI} \) of the 1st integrator are sized to get the thermal noise level lower than the expected resolution. Let \( SNR_{\text{required}} \) be the required signal to noise ratio (SNR) for the converter, \( P_s \) the signal power and \( P_{th} \) the thermal noise power, then

\[
10 \log \left( \frac{P_s}{P_{th}} \right) > SNR_{\text{required}} \tag{1}
\]

where

\[
P_{th} = \frac{4K_B T}{C} \tag{2}
\]
\[
P_s = \frac{A^2}{2} \tag{3}
\]

with \( K_B \) the Boltzman constant, \( T \) the temperature in Kelvin and with \( A \) the sinusoidal input signal amplitude.

This gives us :

\[
C_{sS/H} > \frac{8K_B T 10^{SNR/10}}{A^2} \tag{4}
\]

At the input of the \( \Sigma \Delta \) modulator, the signal is oversampled by a factor \( N \) and if the digital filter removes the out of band noise without any amplification, the effective thermal noise power will be then reduced by a factor \( N \). On the other hand, since the interpolation is performed by adding zeros, and the digital filter has no amplification gain, the signal power is decreased by \( N \) also.

\[
P_{th} = \frac{4K_B T}{C \cdot N} \tag{5}
\]
\[
P_s = \frac{A^2}{2 \cdot N} \tag{6}
\]

It results in

\[
C_{sI} > \frac{8K_B T 10^{SNR/10}}{A^2} \tag{7}
\]

For example, for a UMTS scenario using 2 channels with an normalized input signal amplitude of 0.35 V and an expected SNR of 83 dB at 300 Kelvin, the sampling capacitors are 54 pF which consume an unreasonable die area.

This new interpolation technique allow to decrease the sampling capacitor size. In fact, with the new interpolation technique, equations
signals for a given \( N, M \) and S/H sampling frequency. Four different S/H sampling frequencies can be achieved: \( f_{op}, f_{op}/2, f_{op}/4 \) and \( f_{op}/8 \). The implemented interpolation operation is based on the common tokening. In fact, each channel has \( N_D \) D-flipflops. These flipflops are placed in series and connected to each other via tri-state cells. The tri-state cell control signals \( K_{1...N_D} \) set the number of flipflops that see the token equal to \( K \). Moreover, the channel flipflop chains are also placed in series and are connected together via another tri-state cell. Its control \( M \) enables or disables the next channel. To explain its operation, an example scenario of \( M = 2 \), \( K = 16 \) and consequently \( N = 32 \) will be considered:

- Once the system is reset, the token ring generator shown in Fig. 6 injects a token at the input of the 1st flipflop of the 1st channel. It consists of a Vdd signal during one clock period. At this point, all flipflop outputs are low.
- One \( T_{op} \) later, \( D_{1.1} \) will be equal to “1” and the rest of the outputs will remain low. The token will then reach the 1st tri-state cell of the 1st channel. Its control signal is at a high level because \( K \) is larger than 1. Consequently, the token will be passed to the 2nd flipflop of the 1st channel.
- At the next clock front, \( D_{1.2} \) will return to “0”. \( D_{1.2} \) will become high and the other flipflop outputs will remain low.
- Similarly, the token will go through flipflops and tri-state cells to reach the 16th tri-state cell of the 1st channel. As \( K = 16 \), the tri-state control will be low and the token will be directed to the flipflop that connects the 1st channel chain to the 2nd channel chain.
- The control of this tri-state cell is high because \( M \) was set to be equal to 2. The token will be directed thereby to the input of the 2nd flipflop of the 2nd channel.
- 16 \( T_{op} \) later, the token will get to the tri-state cell that connects the 2nd channel chain to the 3rd channel chain. However at this time, its control signal will be low. The token will then be directed to the token ring generator that will introduce a new token at the 1st channel input.

In the meantime, the flip-flop outputs are recovered in OR networks to generate Multiplexers clock signals \( \Phi_{1...SSd} \) and \( \Phi_{1...ZSd} \). At \( \Phi_{1...SSd} \) clock front a signal sample is processed and at \( \Phi_{1...ZSd} \) clock front samples of value ‘zero’ are obtained. As said before, when sampling at \( f_{op} \), the 1st channel performs its interpolation by a factor \( N \) by adding the first \( K \) signal samples followed by \( N-K \) zeros. Meanwhile when sampling at \( f_{op}/2, K/2 \) samples are acquired during \( K.T_{op} \). Therefore, the even samples are replaced by zeros. Similarly, the modulo 2 to 4 signal samples when sampling at \( f_{op}/4 \)
Time(ns)
RESET
0 50 100 150 200 250 300
0.0
0.2
0.4
0.6
0.8
1.0
1.2
φSD
φ1−ZSD
φ4−ZSD
φ3−ZSD
φ2−ZSD
φ1−SSD
φ2−SSD
φ3−SSD
φ4−SSD
[1x35]0.0
[1x43]0.2
[1x52]0.4
[1x61]0.6
[1x70]0.8
[1x87]1.2
[1x139]0.0
[1x147]0.2
[1x156]0.4
[1x165]0.6
[1x174]0.8
[1x191]1.2
[1x251]0.2
[1x260]0.4
[1x346]0.0
[1x355]0.2
[1x381]0.8
[1x390]1.0
[1x450]0.0
[1x459]0.2
[1x485]0.8

and the modulo 2 to 8 signal samples when sampling at \( f_{op}/8 \), are replaced by zeros.

To create these clock signals, the modulo 8 flip-flop outputs of each channel are firstly ORed together:

\[
OR_i,j = \sum_{k=0}^{3} D_i(j+8k)
\]

For example, the OR output of ( \( D_{1,1}, D_{1,9}, D_{1,17} \) and \( D_{1,25} \)) will be referred to as \( OR_{1,1} \), \( (D_{1,2}, D_{1,10}, D_{1,18} \) and \( D_{1,26} \)) as \( OR_{1,2} \) and so on. The 4 clock signals are generated as follows:

- For a sampling frequency of \( f_{op}/8 \), the \( i \)th channel \( φ_{i-SSD} \) is given by:

\[
f_{op}/8 \ φ_{i-SSD} = OR_{i,1} \bullet φ_{SSD}
\]

In fact, the token reaches \( D_{1,9} 8 \ T_{op} \) after reaching \( D_{1,1} \) creating thereby a clock signal having a front every \( 8 \ T_{op} \). This will allow us to get the signal samples every \( 8 \ T_{op} \) as desired:

- \( f_{op}/2 \ φ_{i-ZSD} = (OR_{i,1} + OR_{i,5}) \bullet φ_{SSD} \)
- \( f_{op}/4 \ φ_{i-SSD} = (OR_{i,1} + OR_{i,3} + OR_{i,5} + OR_{i,7}) \bullet φ_{SSD} \)
- \( f_{op} \ φ_{i-SSD} = \sum_{k=1}^{8} (OR_{i,k}) \bullet φ_{SSD} \)

The \( \bullet \) and the + stand for an AND and OR operations respectively.

During sampling phases, the integrator sampling capacitor must either store signal samples or zeros therefore \( φ_{i-ZSD} \) is the conjugate of \( φ_{i-SSD} \) when \( φ_{SSD} \) is high.

Fig. 7 shows the four channel clock signals in a \( f_{op}/2 \) case obtained with electrical simulations.

IV. Prototype

A 4 channel prototype (Fig. 8) has been designed in a 1.2 V 65 nm CMOS process. The chip total die area including the IO ring is 3 mm². The specifications for each standard are presented in Table I. They were chosen as a compromise of power consumption and robustness.

The architecture of the sigma-delta modulator implemented is a 4th order General Multi Stage Closed Loop (GMSCL)[6] with 2.5 bits level DAC. This structure does not need digital pre-filtering to cancel first stage quantization noise as is the case in traditional cascade \( \Sigma \Delta \).

### Table I

<table>
<thead>
<tr>
<th>Standard</th>
<th>( f_s ) (MHz)</th>
<th>SNR (dB)</th>
<th>M</th>
<th>N</th>
<th>Modulator order</th>
<th>( f_{op} ) (MHz)</th>
<th>( P ) (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GSM/EDGE</td>
<td>0.27</td>
<td>80</td>
<td>1</td>
<td>96</td>
<td>2</td>
<td>208</td>
<td>3.108</td>
</tr>
<tr>
<td>UMTS/DVBT</td>
<td>8</td>
<td>80</td>
<td>2</td>
<td>52</td>
<td>4</td>
<td>208</td>
<td>59.2</td>
</tr>
<tr>
<td>WCDMA/WiMax</td>
<td>25</td>
<td>52</td>
<td>4</td>
<td>32</td>
<td>4</td>
<td>208</td>
<td>110.4</td>
</tr>
</tbody>
</table>

The interpolation network die area is 0.01 mm² and its consumption is 0.32 mW for a \( f_{op} = 208 \) MHz. This represents only a 15% die increase and a 10% power consumption increase compared to the interpolation network required for the classical technique. Nine external control bits are used to fix \( M, K \) and the sampling rate. There are 32 D-flipflops per channel to have \( N \) up to 128 when 4 channels are used. The analog circuit will not be presented in this paper but it is important to note that when \( M \) is lower than four, the inactive channels are turned-off by switching off the biasing current of their OpAmps. \( C_{SS/H} \) was downscaled from 54 pF to 8 pF and \( C_{f} \) to 600 fF.

**Conclusion**

This paper has proposed a new interpolation technique based on oversampling the input signal. It reduces capacitor sizes and consequently the required die area compared to the one required by classical interpolation by zeros. Besides, this new technique decreases the order of the required AAF.

This new interpolation technique was employed in a 4 channel \( T1\Sigma\Delta \) prototype designed in 1.2 V 65 nm CMOS process.

**References**