A General Cost-effective Design Structure for Probabilistic-Based Noise-Tolerant Logic Functions in Nanometer CMOS Technology

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Abstract—Noise-immunity of a logic gate or a circuit is now an important design criterion with dimension scaling to nanometers. Two noise-immune design structures based on Markov random field (MRF) have been proposed in [1], [2] and [3]. These design structures can achieve an excellent noise-immunity but with a large number of redundant transistors. In this paper, a general noise-immune design structure easy to implement has been proposed. It can achieve nearly the same noise-immunity as Master-and-Slave MRF (MAS-MRF) [3] but with a significantly less area penalty. Basic logic gates are simulated and comparison of different circuits based on different design structures is presented. These simulations are based on the Berkeley Predictive Technology Model (BPTM) 65nm CMOS Technology [4] and ST 65nm CMOS models.

Index Terms—Markov random field (MRF), noise-immunity, general cost-effective structure, CMOS

I. INTRODUCTION

The CMOS dimension scaling technology has dramatically improved the performances of transistors and devices in the past decades. In order to keep the power dissipation constant or at a low degree, the supply voltage should scale linearly with the size [5]. In this situation, the reduction of noise margin makes the transistors and devices working in a noisy signal environment. As a result, the transistors in nanometers are much more prone to soft errors, and thus the noise-immune ability of a logic gate or a circuit becomes an important design criterion [6].

For the intrinsic random nature of noise, traditional fault-tolerant design methodologies based on hardware redundancy, e.g., Triple-Modular-Redundancy (TMR) [7], Cascade TMR (CTMR) [8], are not capable to obtain noise-immunity. The noise interferes the input signal of each module and degrades the right judgment of the majority voter. The NAND-multiplexing methodology proposed by Von Neumann [9] can produce the reliable result using unreliable components. However, it needs an extremely high degree of redundancy [10]. The reconfiguration technology is more effective to deal with manufacturing defects or permanent faults and requires enormous amounts of redundancy [11].

Therefore, the traditional approaches are not effective to attain noise-immunity for the random and dynamic nature of noise. Probabilistic-based technologies are more suitable to deal with this problem [12], [13], [14]. One of the promising noise-tolerant probabilistic-based designs is proposed in [1], which is based on Markov random field (MRF) [15]. According to Nepal et al. [1], the reliability or the noise-immunity of a circuit can be improved by maximizing the joint probability of valid input-output pairs with a cost of hardware redundancy. Furthermore, it was optimized in [2] in order to reduce its area penalty. In [3], a Master-and-Slave MRF (MAS-MRF) design structure was proposed by Wey et al., which can obtain nearly the same noise-immune ability as structures in [1], [2] but with fewer transistors. In addition to the area over-cost, another disadvantage of approaches proposed in [1], [2], [3] is that they did not propose a general design structure applicable to all the basic logic gates. In other words, we should design every single logic gate specially. Also another approach based on MRF was proposed in [16], which is based on Differential Cascode Voltage Switch (DCVS). However, this methodology is just desirable for an inverter.

In this work, we propose a general cost-effective noise-immune design structure of logic functions. Compared with MAS-MRF structure, our proposed structure can be implemented to all the basic logic gates with nearly the same noise-immune ability and a much less area cost. Furthermore, this generality means that the proposed structure applies also for functions involving several logic gates and is therefor much more cost effective than the solutions mentioned before. This paper is organized as follows. Section II reviews the preliminaries on MRF theory and the previous noise-immune circuit design structures. The proposed design structure is described in Section III. Section IV shows the simulation results and comparisons of different design structures. Simulations have been done in SPICE using the Berkeley Predictive Technology Model (BPTM) 65nm CMOS Technology [4] and in Spectre based on ST 65nm CMOS models. Finally, discussions and conclusions are given in Section V.

II. PRELIMINARIES ON MRF THEORY AND REVIEW OF PREVIOUS NOISE-IMMUNE CIRCUIT DESIGN STRUCTURES

A. Preliminaries on MRF Theory

Define a set of random variables as \( x = x_0, x_1, \ldots, x_k \). Each variable \( x_i \) can take various values from a value set \( \Omega \),
which can be defined either continuous or discrete according to the model requirements. In special cases (e.g., digital circuit design), $\Omega = \{0, 1\}$. Each variable $x_i$ has a neighborhood defined as $A_i$, $A_i \in \{X - x_i\}$. Take the graph shown in Fig. 1 as an example. In this case, $x_0$ has a neighborhood $A_0 = \{x_1, x_2, x_3\}$, and $x_1$ has a neighborhood $A_1 = \{x_0\}$. The combination of a variable $x_i$ and its neighborhood $A_i$ is called a clique from the graph view. The cliques combination is denoted as $C$ and $c$ is a subset of $C$.

![Fig. 1. A simple Markov random field graph.](image)

If $\chi$ satisfies the following conditions, $\chi$ is called a Markov Random Field (MRF) [15]:

$$P(x_i = o_i) > 0, \forall x_i \in \chi, \exists o_i \in \Omega \quad (1)$$

$$P(x_i = o_i|\chi - x_i) = p(x_i = o_i|A_i) \quad (2)$$

According to the definitions, “positivity” (1) and “Markovianity” (2) respectively, the conditional probability of a variable only relies on its own neighborhood.

For a given MRF $\chi$, the joint probability can be expressed as

$$p(\chi) = p(x_1, x_2, \ldots, x_k) \quad (3)$$

where $x_i \in \chi$, $i = 1, 2, \ldots, k$.

It is difficult to calculate equation (3) directly, especially when $\chi$ contains a large number of variables. However, as pointed out by Hammersley-Clifford theorem [17], the joint probability can be formulated as

$$p(\chi) = \prod_{c \in C} F_c(x_c) \quad (4)$$

Here $F_c(x_c)$ is called Gibbs energy function and stands for the joint probability of a clique of variables. An explicit expression of $F_c(x_c)$ is given by the Gibbs distribution in

$$F_c(x_c) = \frac{1}{Z} e^{-\frac{U(x_c)}{k_b T}} \quad (5)$$

where $Z$ is the normalization constant to make the summation of $F_c(x_c)$ equal to 1. $U(x_c)$ is the clique energy and depends only on the variables of clique $c$. $k_b$ is the Boltzmann constant and $T$ is the temperature.

### Table I

<table>
<thead>
<tr>
<th>$x_0$</th>
<th>$x_1$</th>
<th>$x_2$</th>
<th>$f(x_0, x_1, x_2)$</th>
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<tbody>
<tr>
<td>0</td>
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</table>

#### B. Previous noise-immune circuit design structures

From equations (3), (4) and (5), it can be deduced that if the temperature is set constantly, a higher $U(x_c)$ will generate a smaller value of energy function $F_c(x_c)$ and consequently a lower joint probability $p(\chi)$. Thus, we can improve the noise-immune ability by minimizing the $U(x_c)$.

Before implementing the noise-immune circuit design, a logic gate or a circuit should be mapped to a MRF graph. In this mapping process, every signal of a circuit should be represented as a variable or a node. If a signal dependence exists between two signals, an edge should be added between the two corresponding nodes graphically. For example, Fig. 2 represents the MRF graph of a two-input NAND gate. All the possible input-output states are described in Table I, where $x_0, x_1$ are the two inputs, $x_2$ is the output and $f(x_0, x_1, x_2)$ represents whether the input-output state is valid or not. If $f(x_0, x_1, x_2) = 1$, it is a reasonable state and, on the contrary, if $f(x_0, x_1, x_2) = 0$ describes an invalid or a false state.

![Fig. 2. The two-input logic NAND gate (left) and its corresponding MRF graph (right).](image)

According to Table I, the valid input-output states are $S(0, 1, 1) = \{001, 011, 101, 110\}$. Thus the energy function of $s_0 s_1 s_2$ can be expressed as the minus summation over minterms of the valid states [1]:

$$U(s_0, s_1, s_2) = - \sum_i f_i(s_0, s_1, s_2)$$

$$= -(s_0 \cdot s_1 s_2 + \overline{s_0} s_1 s_2 + s_0 \overline{s_1} s_2 + s_0 s_1 \overline{s_2}) \quad (6)$$

In order to map the MRF to a noise-immune circuit, we follow three steps [1]:

- Step 1: for each variable $x_i$, a bistable storage element should exist with the value of “0” and “1”;

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TABLE I

<table>
<thead>
<tr>
<th>All the possible input-output states of a two-input NAND gate</th>
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<tbody>
<tr>
<td>$x_0$</td>
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<td>0</td>
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Step 2: each valid state in equations (6) should be generated;
Step 3: a feedback loop should exist for each valid state to enhance its stability, consequently maximizing the joint probability of correct logical values.

Take the mapping of a logic NAND gate as an example. Three variables exist here: \( x, y, z \). As the feedback loop, which reduces the transistor number and the valid states with the output value 1, then each valid state should be generated by a combinational sub-circuit and finally the feedback loops enhances the valid states. The circuit diagram of a noise-immune NAND is presented in Fig. 3.

According to the Boolean simplification and valid minterms reduction, an optimized expression of equation (6) is given as:

\[
U(s_0, s_1, s_2) = - \sum_i f_i(s_0, s_1, s_2) \\
= -(\bar{s}_0 \cdot \bar{s}_1 s_2 + \bar{s}_0 s_1 s_2 + s_0 \bar{s}_1 s_2 + s_0 s_1 \bar{s}_2) \\
= -((\bar{s}_0 + \bar{s}_1)s_2 + (s_0 s_1)\bar{s}_2)
\]

(7)

According to equation (7), Nepal et al. optimized the generation of the valid states and thus reduced the transistor numbers, as proposed in [2].

Another design structure is MAS_MRF [3]. Its structure is shown in Fig. 4. The Master subset generates the valid states and the Slave subset is the feedback loop. The Master subset divides the valid states into the valid groups “0” and “1”. All the valid states with the output value 1 compose the “1” group and those with output value 0 compose “0” group. Compared with [1], another advantage of MAS_MRF is the redesign of the feedback loop, which reduces the transistor number and the hardware complexity.

For example, for a MAS_MRF NAND logic gate, the minterms with \( s_2 \) belong to group “1” and the minterms with \( \bar{s}_2 \) belong to group “0”. It reduces the valid states generator from four NAND gates in Fig. 3 to one NAND gate, one NOR gate plus two inverters. As for the feedback loop, it contains only two NAND gates and two inverters while in Fig. 3, five NAND gates and seven inverters are required. The MAS_MRF NAND gate is presented in Fig. 5.

III. PROPOSED GENERAL LOGIC GATES DESIGN STRUCTURE

We propose a general Cost-Effective Noise-Tolerant circuit design structure based on Markov Random Field, named CENT_MRF. In order to illustrate the proposed approach, take account of the NAND gate. Its corresponding energy function is given in equation (7). We know that

\[
\bar{s}_0 + \bar{s}_1 = s_0 s_1
\]

(8)

Thus, equation (7) can be formulated to:

\[
U(s_0, s_1, s_2) = -((\bar{s}_0 + \bar{s}_1)s_2 + s_0 s_1 \bar{s}_2) \\
= -(s_0 s_1 s_2 + s_0 s_1 \bar{s}_2) \\
= -(F_{NAND}(s_0, s_1) s_2 + F_{NAND}(s_0, s_1) \bar{s}_2)
\]

(9)

where \( F_{NAND}(s_0, s_1) \) is the logic function of a NAND gate. Its input signals are \( s_0, s_1 \) and its output signal is \( s_2 \).

We propose to proceed in the same way to obtain the energy function of any logic gate. Especially, this produces the energy function for the basic logic gates as shown below.
• For an inverter:
\[ U(s_0, s_1) = -(s_0 s_1 + s_0 s_1) = -(F_{INV}(s_0) s_1 + F_{INV}(s_0) s_1) \] (10)

• For a NOR gate:
\[ U(s_0, s_1, s_2) = -(s_0 s_0 s_2 + (s_0 s_1 + s_0 s_1 + s_0 s_1) s_2) = -(F_{NOR}(s_0, s_1) s_2 + F_{NOR}(s_0, s_1) s_2) \] (11)

• For a XOR (exclusive-or) gate:
\[ U(s_0, s_1, s_2) = -((s_0 s_1 s_2 + (s_0 s_1 + s_0 s_1 + s_0 s_1) s_2) = -(F_{XOR}(s_0, s_1) s_2 + F_{XOR}(s_0, s_1) s_2) \] (12)

The expression of the energy function for a general logic combinational function can be straightforwardly given as
\[ U_{comb}(s_0, s_1, \ldots, s_{n-1}, s_n) = -(F_{comb}(s_0, s_1, \ldots, s_{n-1}) s_n + F_{comb}(s_0, s_1, \ldots, s_{n-1}) s_n) \] (13)

where:
• \( F_{comb}(s_0, s_1, \ldots, s_{n-1}) \) describes the logic combinational function,
• \( s_0, s_1, \ldots, s_{n-1} \) present the input signals,
• and \( s_n \) is the output signal of the gate.

Based on expression (13), the general CENT_MRF structure for a logic combinational function is obtained as Fig. 6, where:
• \( T_{comb} \) stands for the target logic combinational circuit,
• \( Inv \) represents a logic inverter,
• \( x_0, \ldots, x_{n-1} \) are the input signals,
• and \( x_n \) are the complementary output signals.

The proposed CENT_MRF structure implementation for a NAND gate is presented in Fig. 7. Supposing that an inverter requires 2 transistors and a NAND gate requires 4 transistors, the area overhead of the proposed structure is only 10 transistors. Compared with MRF NAND gate (Fig. 3) and MAS_MRF NAND gate (Fig. 5), the proposed noise-tolerant NAND gate reduces the number of transistors from 60 to 14 (a 76.67% reduction) and from 28 to 14 (a 50% reduction), respectively. Note that this overhead is constant and independent of the target logical function \( T_{comb} \).

IV. NOISE-IMMUNITY SIMULATION RESULTS OF DIFFERENT DESIGN STRUCTURES

A. Quantifying the noise-immunity

In order to quantify the noise-immunity of different design circuits, we adopt the Kullback-Leibler distance (KLD) [18]. It quantifies the similarity of two different signals through comparing the discrepancy between the signal probabilities \( P_{real} \) and \( P_{ideal} \). Here \( P_{real} \) is the signal probability of the actual output, and \( P_{ideal} \) is the signal probability of an ideal output. KLD is defined as
\[ KLD(S_{ideal}, S_{real}) = \sum_{\text{states}} P_{ideal} \log_2 \left( \frac{P_{ideal}}{P_{real}} \right) \] (14)
where \( \text{states} \) specify the logic states of a signal.

For a output signal of a logic gate or a circuit with two states 0 and 1, KLD can be given in
\[ KLD(S_{ideal}, S_{real}) = P_{ideal_0} \log_2 \left( \frac{P_{ideal_0}}{P_{real_0}} \right) \]
\[ + P_{ideal_1} \log_2 \left( \frac{P_{ideal_1}}{P_{real_1}} \right) \] (15)
where \( P_{ideal_0}, P_{real_0} \) are the probabilities of signal 0 and \( P_{ideal_1}, P_{real_1} \) are the probabilities of signal 1.

It is easy to calculate the ideal signal probabilities of a logic gate or a circuit from its truth table. For the actual circuit, with its output signal probability contaminated by the noise, we sample the output signal at discrete points and evaluate its signal probabilities. According to the Nyquist Shannon sampling theorem [19] [20], the Nyquist rate should be at least two times higher than the highest signal frequency. In ours simulations, the smallest time period of input signals is 0.5 \( \mu \)s and the discrete points are sampled every 1 \( \mu \)s. This means the sampling rate is 0.5 \( \times 10^6 \) = 500 times higher than the highest signal frequency. Thus these sampled discrete points can accurately represent the original signal. The smaller the
KLD is, the more similar these two signals are. When KLD equals to 0, we can treat the actual output as ideal.

B. Simulation results (SPICE)

In this work, several logic gates using the proposed CENT_MRF structure have been simulated. Among them, we can find an inverter, a multiple-input NAND gate, the two-input NOR, the two-input XOR. The simulations were realized in SPICE using the Berkeley Predictive Technology Model (BPTM) 65nm CMOS Technology [4] at 100°C. The supply voltage was set to $V_{dd} = 0.15V$, and the threshold voltage was set to 0.2V for NMOS and -0.22V for PMOS. A Gaussian white noise with the 60mV root mean square (RMS) standard deviation was generated and added to the input signal, just the same as [1] and [2]. Fig. 8 illustrates the simulation process.

Fig. 8. The simulation process of a general logic combinational circuit.

Because of the limited space, only the simulation results of a two-input NAND gate is presented in Fig. 9.

C. Simulation results (SPECTRE)

Spectre simulator has been used for simulations of basic logic gates as well as more complex logic combinational functions such as a one-bit full-adder (FA), a four-bit Ripple Carry Adder (RCA) and a (8, 4) Hamming Decoder to compare the noise-immunity of different design structures. We used the low threshold voltage and low power PMOS (plvtlp) and NMOS (nlvtlp) transistors of ST 65nm library. The supply voltage of the gates is 1.2V and the temperature is 25°C. Different input signals with different signal-noise-ratio (SNR) were simulated and KLDs of output signal were quantified. If there were more than one output in the circuit, the output signal of deepest-path was treated as the representation.

The simulation results are shown in Fig. 10 to Fig. 14. Table II shows the comparison of the transistor number for different bench circuits.

V. DISCUSSIONS AND CONCLUSIONS

This paper proposed a general cost-effective noise-tolerant circuit structure based on Markov Random Field. It is a general design approach easy to implement for all logic combinational functions. Simulations were realized with the Berkeley Predictive Technology Model (BPTM) 65nm CMOS Technology [4] and ST 65nm CMOS models. From Fig. 9 to Fig. 14 and Table II, we can conclude that proposed CENT_MRF design
TABLE II
TRANSMITTER NUMBERS FOR DIFFERENT BENCH CIRCUITS

<table>
<thead>
<tr>
<th>Bench circuits</th>
<th>MRF</th>
<th>Master and Slave MRF</th>
<th>Proposed CENT_MRF</th>
<th>Transistor Number Reduction</th>
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<tr>
<td></td>
<td>[1]</td>
<td>[3]</td>
<td>[1]</td>
<td>[3]</td>
</tr>
<tr>
<td>2-input NAND</td>
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<td>28</td>
<td>14</td>
<td>76.67%</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>50%</td>
</tr>
<tr>
<td>3-input NAND</td>
<td>144</td>
<td>34</td>
<td>16</td>
<td>88.89%</td>
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<td>52.9%</td>
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<td>4-input NAND</td>
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<tr>
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<td>1-bit full-adder</td>
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<tr>
<td>4-bit RCA</td>
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<td>648</td>
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<tr>
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<td>50%</td>
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</table>

Fig. 12. The KLDs of different design structures of a four-bit RCA.

Fig. 13. The KLDs of different design structures of a two-input XOR gate.

structure can obtain nearly the same or even better noise-immunity but with less area penalty. Compared with original MAS_MRF, the area cost can be reduced 50% for a single two-input NAND gate, 50% for a RCA and 33.3% for a (8, 4) Hamming Decoder. The future work will focus on the structure for multiple-output gates and the mapping optimization for large circuits, especially for selective implementation. Other design criteria should be taken into account, e.g., the time delay, the power consumption, the transistor threshold voltage variation, etc. Also the bit-error-rate (BER) of some application-related circuits should be tested to quantify the noise-immunity more accurately.

Fig. 14. The KLDs of different design structures of (8, 4) Hamming Decoder.

REFERENCES


