Fully Digital Feedforward Background Calibration Of Clock Skews For Sub-sampling TIADCs Using The Polyphase Decomposition

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Abstract—This paper presents a low-power fully digital clock skew feedforward background calibration technique in sub-sampling Time-Interleaved Analog-to-digital Converters (TIADCs). Both estimation and correction algorithms share the common derivative filter, which enable to save filter hardware. Furthermore, these algorithms use the polyphase filtering technique and do not use the adaptive digital synthesis filters. Thus, the proposed calibration can be implemented at a moderate hardware with low power dissipation. The adopted feedforward technology eliminates the stability issues encountered with the adaptive technique. The Hardware Description Language (HDL) design of the proposed calibration is synthesized using 28nm FD-SOI process for a 60dB SNR TIADC clocked at 2.7GHz. The calibration is designed for both baseband and sub-sampling TIADC applications. The synthesized calibration system occupies 0.04mm² area and dissipates 33.2mW total power for sub-sampling ADC with the input at the first four NBs; and it obtains 0.02mm² chip area occupation and 15.5mW power consumption for the Nyquist TIADCs.

Index Terms—All-digital feedforward calibration, Subsampling and undersampling TIADCs, FPGA/ASIC implementation, polyphase filtering.

I. INTRODUCTION

In modern communication systems such as broadband satellite receivers, cable TV tunners and Software-Defined Radios, Analog to Digital Converters (ADCs) play an essential role. Such ADCs require very high sampling rates with high resolution and low power dissipation. A Time-interleaved ADC (TIADC) which is formed by several slow but accurate ADCs in parallel, is a promising solution to achieve these goals [1], [2]. Unfortunately, the TIADC performance suffers from the channel mismatches including offset, gain and timing mismatches due to process, voltage, and temperature variations. These channel mismatches produce frequency aliases on the output signal and, hence, degrade the Signal-to-Noise and Distortion Ratio (SINR) and Spurious-Free Dynamic Range (SFDR) performance of the converters significantly. Among these aforementioned errors, sample-time errors are the most critical as the timing mismatch errors increase with the input frequency and overshadow the effect of other mismatches for broadband inputs [3]. For these reasons, this framework focuses on tackling the timing mismatch problem.

The timing mismatches in TIADCs can be effectively handled by analog and/or mixed signal calibration techniques [1], [4]–[9]. Mixed-signal calibration techniques mitigate the clock skew effect by adjusting the variable-delay line in clock buffers. They exhibit good performance but the analog correction schemes limit the overall ADC resolution due to process, supply voltage and temperature variations and a thermal noise. Moreover, they require an additional analog circuit with longer development time and are not portable between CMOS technology nodes.

Recently technology shrinking, fully digital techniques seem to be a more promising solution to overcome the above issues of the analog and mixed-signal calibration. They can be developed faster, make use of the advantages of CMOS technology scaling, and easier to port to the next technology generation. Most calibration approaches [10]–[17], are derived assuming an input signal band-limited to the Nyquist frequency, i.e., the input located in the first Nyquist Band (NB), also commonly known as Nyquist Zone (NZ). However, these techniques cannot be directly applied in the undersampling (or subsampling) TIADCs which samples the band-limited signals in the higher NB and is an interesting solution in the next generation directly sampling receivers such as sub-sampling receivers, software defined radios, and broadband satellite receivers [18], [19]. A few all-digital calibration techniques coping with mismatches in undersampling TIADCs have been proposed in [19]–[22]. Nevertheless, they require either an additional channel [21] or a pilot input signal [22] for calibration. The work in [20] is performed with the assumption of narrow-band signals and applied for only two channels. For the very high speed applications, the calibration in [19] used the polyphase filtering technique in order to enhance the working frequency of the Digital Signal Processing (DSP) units. However, usage of two identical derivative filters (one in correction and one in estimation) is not optimal in term of power consumption. In order to save the filter hardware, sharing one ideal differentiator filter between correction and estimation schemes is actually proposed in this framework.

Regarding the all-digital calibration implementation, calibration schemes are performed either with the aid of a feedback loop as shown in Fig. 1(a) or in a feedforward manner as shown in Fig. 1(b) [23]. Therefore, the former is defined as all-digital feedback calibration and the latter as all-digital feedforward calibration. Most prior arts [11]–[17], [19]–[22] used adaptive feedback techniques which suffer from the potential stability issues [10], [24]. In order to overcome these issues and to achieve the low power dissipation, the calibration algorithms in [10], [25] are performed in feedforward manner. This approach indeed calculated the cross-correlations among the adjacent sub-ADCs and the cross-correlations between the sub-ADC output samples and their corresponding derivative.
samples. Using orthogonal property of input signal and its derivative, these cross-correlations enable a direct estimation of clock skews. The above pairwise cross-correlations are achieved by using the overall TIADC output and a FIR filter whose coefficients are \((-1, 0, +1)\). The sub-ADC derivative is obtained by feeding the TIADC gain-corrected samples into a FIR baseband derivative filter [10]. With such implementation, the used FIR filters are required to run at full sampling rate, which is very challenging and power hungry for very high speed ADC design. Moreover, this technique does not work with input at any NZ.

Inspired by the all-digital feedforward calibration scheme of timing mismatch proposed in [10], [25], in this paper, we present its theoretical analysis for sub-sampling TIADCs in any Nyquist Band. In addition, the complexity of the estimation scheme is reduced by using one cross-product between the sub-ADC output and the output derivative of the adjacent sub-ADC instead of using two cross-products in the computation of the derivative of the input autocorrelation. Furthermore, we leverage our previous work [19] by using polyphase implementation for both estimation and correction algorithms to reduce the power. Finally, the digital feedforward background calibration system is synthesized in 28nm FD-SOI process.

In detail, a linear equation system of the clock skews is derived from the pairwise cross-correlations of sub-ADC outputs which are obtained from the direct sub-ADC output samples. Solutions of these established equations are the clock skew estimates. In addition, in both correction and estimation schemes, the derivatives of sub-ADC outputs are required and computed by using polyphase technique. Note that the estimation and correction algorithms run at the sub-ADC rate, leading to the lower power consumption. They are also share the same derivative filter, i.e., the proposed algorithm saves one derivative filter in comparison with our previous works proposed in [19], [26]. Furthermore, they do not use the adaptive filter banks. As a result, the proposed calibration alleviates the power consumption and chip die area. It is also employed for very high speed (beyond several gigahertz) TIADC design.

The rest of the paper is organized as follows. Section II reviews time-interleaved ADCs, their limitations and timing skew induced errors. Section III presents the proposed feedforward calibration of the timing offset including the correction and estimation. In order to show the efficiency fo the proposed calibration, section IV analyzes the simulation results, ASIC synthesis results and simulation results post-processing the real data captured from the ADC chip. Conclusions are finally drawn in section V.

II. TIME-INTERLEAVED CONVERTERS

Fig. 2 shows a simplified block diagram architecture of \(M\)-channel TIADCs. It encompasses an analog demultiplexer at the input, a digital Multiplexer (MUX) at the output and \(M\) channel converters with the same sampling period of \(MT_s\). The sampling instant deviation of the neighboring sub-ADCs is \(T_s\). During operation, each selected sub-ADC by the demultiplexer sequentially sampled and digitized an analog input signal \(x(t)\) to form the digital streams. The digital data streams from \(M\) sub-ADCs are then periodically multiplexed by MUX to generate a TIADC digital output \(y[n]\). With time-interleaving technique, the overall sampling rate \(f_s\) of TIADCs ideally is \(M\) times higher than the sampling rate of sub-ADCs. The equivalent sampling period of the TIADCs is \(T_s\).

![Fig. 2: \(M\)-channel TIADCs: (a) Block diagram and (b) timing diagram](image-url)

However, channel mismatches among the constituent sub-ADCs including offset, gain and timing mismatches significantly degrade the linearity performance of TIADCs [3]. Offset mismatches creates additive tones at frequency \(k f_{in}\) where \(k\) is integer. The effect of gain mismatch causes amplitude modulation of the input samples, producing scaled replicas of the input spectrum to appear centered around integer multiples of \(f_{in}/M\) (or \(\pm f_{in} + k f_{in}/M\)) where \(f_{in}\) is the input frequency. Both offset and gain errors are static and input frequency independent [5], [27]. The timing mismatch results in phase shift (phase modulation) of the input samples. Clock skew
mismatch creates the scaled copies of the derivative of the input signal spectrum at the first order when timing mismatches are small. These copies locate at the same frequencies as the spurious components stemming from gain mismatch, hence considerably degrading SNDR/SFDR.

As stated in Section I, we focus on the timing mismatches problem in this framework. We assume that there are no gain/offset mismatches and assume $\delta t_i$ is the clock skew (or deterministic relative timing deviation) of the $i$th channel ADC. Ignoring quantization effects, the digital output sequence $y_m[k]$ of the $m$th channel ADC is expressed by

$$y_m[k] = y_m(kT_s) = x(kMT_s + mT_s + t_0 + \delta t_m), \quad (1)$$

where $t_0$ is the initial sampling phase.

The $m$th channel sub-ADC output can be expressed as a sum of an ideal signal and an error term proportional to the timing offset and the signal derivative as [4], [10], [13]

$$y_m[k] \approx x_m[k] + \delta t_m x'_m[k], \quad (2)$$

where $x'_m[k]$ is the derivative of the input signal at the nominal sampling time (or the derivative of sub-ADC output in the case without timing skews). The timing skew induced error is a product of the derivative signal of sub-ADC output samples and its corresponding clock skews.

III. PROPOSED CALIBRATION TECHNIQUE

The proposed calibration for input at the first NZ consists of two main algorithms: correction and estimation presented hereafter. The proposed calibration extension to input at any NZ is described straightforward.

A. Digital Correction

Once the estimates of $\delta t_m$ is known, it can be used in various different ways to get the correct value of the input signal at the nominal sampling time. Some approaches are to use a digital synthesis filter bank in the correction as in [14], [20] that runs at full speed all the time and require large amount of computation resource. Therefore, these approaches are not very suitable for low power specifications. In this framework, the adopted approach is to just subtract the error given by the second term of (2) from the conversion result. This would require a knowledge of the derivatives $x'_m[k]$ of ideal sub-ADC outputs. In blind calibration, the input is unknown, i.e., $x'_m[k]$ is also unknown. Thus, the derivatives $y'_m[k]$ of the distorted sub-ADC output samples are used for correction as done in [10], [11], [13], [24], [27]. Derivatives $y'_m[k]$ are computed in digital domain using polyphase filters of the digital differentiators proposed in [19], [26]. With 25-tap FIR differentiator used in [26], the derivative span is extended up to 90% of the Nyquist zone before it rolls off.

B. Digital Estimation

Let the input analog signal $x(t)$ be Wide-Sense Stationary (WSS) random process and band-limited to the Nyquist frequency, i.e., its mean $E\{x(t)\}$ is constant and its autocorrelation $R_x(\tau)$ depends only the time shift $\tau = t_1 - t_2$ [28]. These characteristics can be expressed by the following equations:

$$E\{x(t)\} = \eta = \text{constant}, \quad (3a)$$

$$R_x(t_1, t_2) = R_x(\tau) = E\{x(t + \tau)x(t)\}, \text{for all } t. \quad (3b)$$

In discrete-time domain, the cross-correlation $R_{fg}[l]$ of two signals $f[n]$ and $g[n]$ is defined by [29], [30]

$$R_{fg}[l] = E\{f[n + l]g[n]\} = \lim_{N \to \infty} \frac{1}{2N + 1} \sum_{n=-N}^{N} f[n + l]g[n], \quad (4)$$

where index $l$ is the (time) shift (or lag) parameter and the notation $R_{fg}[l]$ is extensively used for writing convenience.

Basic idea: To estimate the clock skews of sub-ADCs, the cross-correlation of two adjacent channels of the TIADC is computed. The difference between two cross-correlation functions produces a linear equation system whose variables are timing skews of the individual channel ADCs. A solution of this linear equation system is the timing skews of sub-ADCs. The estimation technique will be interpreted in more detail as follows.

1) Linear Equation System With Clock Skew Variables: From (4), (1) and (3b), the cross-correlation between two consecutive channel ADCs (ADC$_m$ and ADC$_{m-1}$ for $1 \leq m \leq M - 1$) is expressed by

$$R_{y_my_{m-1}}[0] = E\{y_m[k]y_{m-1}[k]\}$$

$$= E\{x(kMT_s + mT_s + t_0 + \delta t_m)$$

$$\times x(kMT_s + mT_s + (m-1)T_s + t_0 + \delta t_{m-1})\}$$

$$= R_x(T_s + \delta t_m - \delta t_{m-1}). \quad (5)$$

Analogously, the cross-correlation of two adjacent sequence outputs from sub-channel ADC$_m$ and ADC$_{m+1}$ for $0 \leq m \leq M - 2$ is written by

$$R_{y_my_{m+1}}[0] = E\{y_m[k]y_{m+1}[k]\}$$

$$= E\{x(kMT_s + mT_s + t_0 + \delta t_m)$$

$$\times x(kMT_s + mT_s + (m+1)T_s + t_0 + \delta t_{m+1})\}$$

$$= R_x(T_s + \delta t_{m+1} - \delta t_m). \quad (6)$$

In order to estimate sample-time errors, the timing error function is defined as the difference of pairwise cross-correlations of sub-ADC output samples and is expressed by:

$$\Gamma_m = R_{y_my_{m-1}}[0] - R_{y_my_{m+1}}[0], 1 \leq m \leq M - 2. \quad (7)$$

By applying the Taylor series expansion up to the first derivative around a zero point, the autocorrelation function $R_x(T_s + \delta t)$ as a function of the variables $\delta t$ is expressed by

$$R_x(T_s + \delta t) \approx R_x(T_s) + \delta t \times \frac{dR_x(T_s + \delta t)}{d\delta t} |_{\delta t = 0} \quad (8)$$

where $R'_x(T_s)$ is the derivative of autocorrelation of the input signal. In practice, the clock skews arising in time-interleaved ADCs are typically small as compared to the sampling interval $T_s$. By Taylor series expansion to (5) and (6) as done in (8), the timing error function $\Gamma_m$ in (7) can be simplified as follows.

$$\Gamma_m \approx R'_x(T_s)(2\delta t_m - \delta t_{m-1} - \delta t_{m+1}), 1 \leq m \leq M - 2. \quad (9)$$
Obviously, (9) is a linear equation system that has \((M - 2)\) linear equations and \(M\) variables being the timing skews of \(M\) channel sub-ADCs. In order to derive the linear equation system having number of linear equations the same as the number of variables, we introduce additionally two timing error functions of \(\Gamma_0\) and \(\Gamma_{M-1}\) as follows.

\[
\begin{align*}
\Gamma_0 &= R_{y_{M-1}y_0}[-1] - R_{y_0y_1}[0], \\
\Gamma_{M-1} &= R_{y_{M-1}y_{M-2}}[0] - R_{y_{M-2}y_{M-1}}[-1].
\end{align*}
\] (10)

By substituting \(m\) for \(m = 0\) into (6), we have

\[
R_{y_{0}y_{1}}[0] = R_x(T_s + \delta t_1 - \delta t_0).
\] (11)

By replacing \(m\) with \(m = M - 1\) into (5), we have

\[
R_{y_{M-1}y_{M-2}}[0] = R_x(T_s + \delta t_{M-1} - \delta t_{M-2}).
\] (12)

Analogously to (5) and (6), we completely compute

\[
R_{y_{M-1}y_0}[-1] = E\{y_{M-1}[k-1] y_0[k]\} = E\{x((k-1)MT_s + (M-1)T_s + t_0 + \delta t_{M-1}) \times x(kMT_s + 0 \times T_s + t_0 + \delta t_0)\} = R_x(T_s + \delta t_0 - \delta t_{M-1}).
\] (13)

From (8), (10), (11), (12) and (13), we have

\[
\begin{align*}
\Gamma_0 &\approx R_x'(T_s)(2\delta t_0 - \delta t_1 - \delta t_{M-1}), \\
\Gamma_{M-1} &\approx R_x'(T_s)(2\delta t_{M-1} - \delta t_{M-2} - \delta t_0).
\end{align*}
\] (14)

From (9) and (14), we have a linear equation system with \(1 \leq m \leq M - 1\) as follows.

\[
\begin{align*}
\Gamma_0 &\approx R_x'(T_s)(2\delta t_0 - \delta t_1 - \delta t_{M-1}) \\
\vdots & \quad \vdots \\
\Gamma_m &\approx R_x'(T_s)(2\delta t_m - \delta t_{m-1} - \delta t_{m+1}) \\
\vdots & \quad \vdots \\
\Gamma_{M-1} &\approx R_x'(T_s)(2\delta t_{M-1} - \delta t_{M-2} - \delta t_0).
\end{align*}
\] (15)

In general, if the derivative of the input autocorrelation \(R_x'(T_s)\) is determined, straightforwardly solving the equation system (15) provides the sample-time error estimates of sub-ADCs.

2) Estimates Of The Input Autocorrelation Derivative:

From (3b), we have

\[
R_x'(T_s) = \frac{dR_x(T_s)}{dT} \bigg|_{T=T_s} = E\{x'(t + T_s)x(t)\}. \tag{16}
\]

Without clock skews, the ideal sampling instant (or the ideal sampling edge) of the \(m^{th}\) sub ADC is at

\[
t_{s_m} = kMT_s + mT_s + t_0, 0 \leq m \leq M - 1.
\] (17)

By replacing \(t\) by \(t_{s_m}\) into (16), we have

\[
R_x'(T_s) = E\left\{x'(kMT_s + (m+1)T_s + t_0) \times x(kMT_s + mT_s + t_0)\right\} = E\left\{x'_{m+1}[k] x_m[k]\right\}, 0 \leq m \leq M - 1.
\] (18)

where \(x_m[k]\) is the ideal output samples of the \(m^{th}\) channel ADC; and \(x_{m+1}[k]\) is the derivative of the desired outputs of the \((m+1)^{th}\) channel ADC. In a blind calibration mechanism, the input signal is not available, i.e., \(x_m[k]\) and \(x_{m+1}[k]\) are unknown. Thus, the output of the sub ADC\(m\) and the derivative of the channel ADC\(m+1\) are used to approximately compute the autocorrelation of the input signal. Thus, the first order derivative of the autocorrelation of the input signal can be computed approximately by

\[
R_x'(T_s) \approx E\left\{y_{m+1}[k] y_m[k]\right\} = R_{y_{m+1}y_m}[0], 0 \leq m \leq M - 1.
\] (19)

In other words, the first order derivative of the autocorrelation of the input signal at the time of \(T_s\) is computed by using one cross-correlation between the sampled output of the \(m^{th}\) channel ADC and the derivative of the output of the \((m + 1)^{th}\) sub-ADC. It has less computation complexity than the approach in [10], [25] where a sum of many cross-correlations is used.

3) Solution Of The Linear Equation System: The linear equation system (15) can be written in matrix notation as follows.

\[
\begin{bmatrix}
\Gamma_0 \\
\Gamma_1 \\
\vdots \\
\Gamma_{M-1}
\end{bmatrix} = \begin{bmatrix}
1 \\
R_x'(T_s)
\end{bmatrix} \approx H \times \delta T,
\] (20)

where \(\delta T\) is a column vector whose elements are individual clock skews of sub-ADCs, and expressed by

\[
\delta T = [\delta t_0, \delta t_1, \ldots, \delta t_{M-1}]^T
\] (21)

and

\[
H = \begin{bmatrix}
2 & -1 & 0 & \cdots & 0 & -1 \\
-1 & 2 & -1 & \cdots & 0 & 0 \\
\vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\
-1 & 0 & 0 & \cdots & -1 & 2
\end{bmatrix}_{M \times M}
\] (22)

is a constant circulant matrix of size \(M \times M\) (\(M\) rows and \(M\) columns) having the following properties.

- If the column index is equal to the row index, its corresponding coefficient is equal to 2.
- If \(\text{ind}_{\text{col}} = \text{ind}_{\text{row}} \pm 1\) modulo \(M\), its corresponding coefficients are equal to -1, where \(\text{ind}_{\text{col}}, \text{ind}_{\text{row}}\) are the index of column and row of matrix \(H\), respectively.
- The coefficients are equal to 0 for all other indexes of the rows and columns.
- \(H\) is a symmetric matrix, i.e., \(H = H^T\), where symbol \(T\) denotes the transpose operator.
- The circulant matrix \(H\) is fully specified by its first row vector. The remaining rows are generated by the cyclic permutations of the first row. The final row is a vector in reverse order compared to the first row. Moreover, both the sum of all rows and the sum of all columns are zero. As a result, the rank of the circulant matrix \(H\) is determined by [31] and is equal to \((M - 1)\).
Taking a sum of all equations of the above linear equation system results in

$$\frac{1}{R_x(T_s)} (\Gamma_0 + \Gamma_1 + \ldots + \Gamma_{M-1}) = 0,$$

(23)

which is not dependent on the variables of \(\delta t_m, 1 \leq m \leq M - 1\). As a result, the linear equation (20) is simplified and expressed in matrix notation by

$$A\delta T = \frac{1}{R_x(T_s)} \Gamma,$$

(24)

where

$$\Gamma = [\Gamma_1, \ldots, \Gamma_{M-1}]^T$$

(25)

and

$$A = \begin{bmatrix}
-1 & 2 & -1 & \cdots & 0 & 0 \\
0 & -1 & 2 & \cdots & 0 & 0 \\
\vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\
-1 & 0 & 0 & \cdots & -1 & 2
\end{bmatrix}_{(M-1) \times M}$$

(26)

is also constant circulant matrix of size \((M - 1) \times M\). The matrix \(A\) is generated by deleting the first row of the constant matrix \(H\). From the properties of matrix \(H\), the circulant constant matrix \(A\) is referred to be full row rank, i.e., \(\text{rank}(A) = M - 1\) [31]. This is equivalent to that the square, \((M - 1) \times (M - 1)\) matrix \(A A^T\) is invertible, meaning that it has full rank, \((M - 1)\) [32]. \(\Gamma\) is a vector of size \((M - 1) \times 1\) in the right-hand side of the linear system (24). A \(M \times 1\) size vector \(\delta T\) is a solution of the equation system (24) if \(A\delta T = \frac{1}{R_x(T_s)} \Gamma\) holds.

The system of linear equations (24) is underdetermined because there are more unknowns (variables \(\delta t_m, 0 \leq m \leq M - 1\)) than equations. This occurs once there are more columns than rows with linearly independent rows. In this case, the least-norm (or least square) solution of the underdetermined system of linear equations is given by authors in [32]–[35]. The unique minimum norm solution (or the unique solution with minimal Euclidean norm) of the system can then be expressed as [32]–[35].

$$\delta T \approx A^T(A A^T)^{-1} \frac{1}{R_x(T_s)} \Gamma.$$  

(27)

\(A^T(A A^T)^{-1}\) is called the pseudo-inverse constant circulant matrix of full rank of \(M\). \(A^\dagger\) is also called a right inverse matrix of \(A\). The elements (or coefficients) of a minimum norm solution vector of the underdetermined equations are the clock skew estimates of sub-ADCs \(\delta t_m, 0 \leq m \leq M - 1\).

C. Architecture Of The Proposed Calibration

The overall architecture of the proposed calibration technique is shown in Fig. 3. It mainly consists of a Derivative Polyphase Filter (DPF) block proposed in [19], a Cross-correction Computation Unit (CCU), a Gamma computation Unit (FU) block, and a Matrix Processing Unit (MPU) block.

- **The Derivative Polyphase Filters (DPF):** From (19) and (2), the derivatives of the sub-ADC outputs are required to estimate the timing mismatch coefficients. The signal derivatives of sub-ADC outputs are obtained by an DPF block. The DPF block encompasses polyphase filter sub-systems subPF\(i\), \(0 \leq i \leq M - 1\) described in [19], [26]. The subPF\(i\) is formed by delay elements \(z^{-1}\) and the type-1 polyphase filter components \(P_i(z)\) of the Nyquist derivative FIR filter. The impulse response of the \(i^{th}\) polyphase filter is given by

$$p_i[n] = h_d[nM + i], i = \{0, 1, \ldots, M - 1\},$$

(28)

where \(h_d[n]\) is the impulse response of ideal derivative filter and expressed as [29], [30]

$$h_d[n] = \begin{cases} 
\frac{\cos(n\pi)}{n} & (n \neq 0) \\
0 & (n = 0)
\end{cases}.$$  

(29)

The architecture of subPF\(i\) is shown in Fig 4 in the detail for an example of two-channel TIADCs. This architecture can be easily extended to \(M\)-channel TIADCs [19], [26].

![Fig. 3: The overall architecture of the proposed calibration](image)

![Fig. 4: Equivalent polyphase structure of the two-channel TIADCs](image)
aging the product of two signals over $N$ samples as [29], [30]  
\[
R_{fg}[l] = E\{f[n+l]g[n]\} = \frac{1}{N} \sum_{n=0}^{N-1} f[n+l]g[n]. \tag{30}
\]

The computation of the expected values in (30) is realized by the CCU block as shown in Fig. 5 for lag $l = 0$, that consists of a multiplier and a Modified Moving Average (MMA) filter [25]. Note that if time shift $l \neq 0$, the delay is added to a corresponding input of multiplier in order to compute the signal $f[n+l]$ with lag $l$. The MMA filter is drawn in Fig. 6. The MPU performs (Smoothing Moving Average) filter is defined by  
\[
s[n] = \frac{N-1}{N} s[n-1] + \frac{1}{N} q[n], \tag{31}
\]
where $s[n]$ and $q[n]$ are its output and input, respectively. It is used to calculate the average of cross-product between two input signals in (30). The differential equation (31) can be simplified by  
\[
s[n] = \frac{1}{N} (q[n] - s[n-1]) + s[n-1]. \tag{32}
\]
As a result, the MMA filter is drawn in Fig. 6. The coefficient $\alpha = \frac{1}{N}$ represents a constant smoothing factor of MMA filter. Number of samples $N$ is selected to be $2^k$ where $k$ is the positive integer since multiplying the signal with $\alpha$ is equivalent to a left arithmetic shift by $k$ places, hence outperforming hardware multipliers.

- **Gamma computation Unit (GU):** $\Gamma U$ consists of the Gamma computation sub-units $\Gamma U_m$ that compute timing error functions $\Gamma_m, 1 \leq m \leq M-1$. From (4) and (7), sub-Unit $\Gamma U_m$ is illustrated in Fig. 7 for $1 \leq m \leq M-2$. From (4) and (10), the sub-Unit $\Gamma U_{M-1}$ is shown in Fig. 8. Sub-Unit $\Gamma U_0$ is not shown herein because the timing error function $\Gamma_0$ is not used for the timing skew estimation, see (25). However, the architecture of $\Gamma U_0$ can be easily derived based on (4) and (10).

- **Matrix Processing Unit (MPU):** The MPU performs the matrix product in (27). The pseudo-inverse constant circulant matrix $A^+$ is referred to be as an input parameter of the proposed calibration algorithm.

- **Correction Scheme:** The corrected samples $\tilde{y}_m[k]$ of the $m^{th}$ sub-ADC are computed by first-order Taylor approximation according to (33). This principle is realized in Fig. 9.  
\[
\tilde{y}_m[k] = y_m[k] - \delta_{t_m} y'_m[k]. \tag{33}
\]

**D. Calibration For Input At Any Nyquist Band**

As elaborated in sections III-B, III-A and III-C, in order to cancel out the timing skew error, the derivative of the WSS input bandlimited to Nyquist frequency is determined by using the polyphase filter decomposition of the ideal differentiator filter with impulse response $h_d[n]$. Let consider a continuous time WSS Bandpass (BP) input signal inside the $k_{NB}^{th}$ NB. Its frequency content in the two frequency bands is then defined by  
\[
(k_{NB} - 1) \frac{f_s}{2} < f_L \leq |f| \leq f_H < k_{NB} \frac{f_s}{2}, k_{NB} \geq 1, \tag{34}
\]
where $f_L, f_H$ are the low and high cutoff frequencies of the input, respectively. This BP input occupied the $k_{NB}^{th}$ Nyquist zone. If the condition (34) is fulfilled, there will be no aliases after sub-sampling the original input [36]. In [19], [27], a
filter is proposed to compute the derivative of the original BP input of undersampling (or sub-sampling) TIADC. The filter is called a BP Derivative (BD) filter and re-sketched in Fig. 10. It encompasses a scaling factor dependent on the order of NB $k_{NB}$ and two Finite Impulse Response (FIR) filters with constant coefficients: a differentiator $h_d[n]$ and a Hilbert filter. The Hilbert filter is an all-pass filter that shifts the input signal phase by 90 degree [36] and its impulse response $h_k[n]$ is expressed by [30], [36]

$$h_k[n] = \begin{cases} \frac{2 \sin^2(\frac{n \pi}{2})}{n} & (n \neq 0) \\ 1 & (n = 0) \end{cases}. \quad (35)$$

The impulse response of the BD filter is expressed by

$$h_{bd}[n] = h_d[n] + h_k[n] \times (-1)^{k_{NB}} \left[ \frac{k_{NB}}{2} \right] 2\pi. \quad (36)$$

The constant (or scale factor) of $(-1)^{k_{NB}} \times \left[ \frac{k_{NB}}{2} \right] \times 2\pi$ is referred to as an input parameter of the proposed calibration algorithm. Given the order of NB, the BD filter has constant coefficients. By decomposing the $M$-component polyphase filter structure for the BD filter $h_{bd}[n]$ as done for the aforementioned differentiator $h_d[n]$, the overall architecture of the proposed calibration illustrated in Fig. 3 is applicable for input at any NBs.

IV. EXPERIMENTAL RESULTS

A. Simulation Results

To verify the efficiency of the proposed technique, simulations were carried out on an undersampling four-channel TIADCs with 60dB SNR (thermal noise level) clocked at $f_s = 2.7$GHz. Timing skews are modeled as Gaussian distribution with zero mean and standard deviation $\sigma_{\text{inc}}$ of 0.33ps. The constant smoothing factor $\alpha$ of MMA filters is chosen as 2$^{-15}$ to achieve a good compromise between the convergence speed and the parameter estimation precision [37]. The order NB $k_{NB}$ of the input is designed up to the fourth Nyquist band for the next-generation sub-sampling radio receivers in order to choose proper and feasible sampling rate [29], [38]. Thus, the simulations demonstrating the efficiency of the proposed calibration are therefore performed up to the fourth NZ i.e., simulations with $k_{NB} = \{1, 2, 3, 4\}$.

The number of FIR taps is designed to be equal for both derivative filter and Hilbert filter. The coefficients of these FIR filters are obtained by multiplying the exact coefficients by Hanning window to mitigate the influence of a truncation error. Their polyphase filters are causal and linear phase FIR filters. The coefficients of polyphase filters are explicitly computed based on equations (28), (29), (35) and (36). Note that constant group delay of the polyphase filter of number of FIR taps $1 + 2M$ plus 1 [19], [19]. The SNDR and SFDR performance versus the FIR taps over the first four NBs is drawn in Fig. 11. The solid and dash-dot curves show the performance with/without calibration, respectively. The curves with $\bigcirc$, $\square$, $\bigstar$ and $\bigtriangledown$ markers show the SNDR/SFDR performance in respect of the first four NZs, respectively. As can be noticed, the optimal number of FIR taps is 25 taps at which the performance saturates.

Fig. 12 shows the output spectrum of TIADC before and after calibration for a single-tone sinusoidal input signal is generated at $f_{in} = 0.45 \times f_s + \frac{f_s}{4}$ in the second NB. As illustrated in Fig. 12(b), the spurs due to the timing skews are mitigated significantly in comparison with the output spectrum before calibration shown in Fig. 12(a). The SFDR is improved by almost 35dB. The SNDR value after calibration is 60dB which is equal to its value in the no-mismatch case. Fig. 13(a) illustrates the convergence speed of timing mismatch estimates. The Monte Carlo simulation method is used to generate the many iterations of clock skews in order to show the convergence speed of SNDR during calibration for the single-tone sinusoid input at frequency of

![Fig. 10: Bandpass derivative filter.](image)

![Fig. 11: SNDR/SFDR performance vs. number of FIR taps.](image)

![Fig. 12: Output spectrum of four channel TIADCs with input](image)
0.45 × \(f_s + (k_{NB} - 1) \times f_s\), \(k_{NB} \in \{1, 2, 3, 4\}\). The SNDR curves as functions of time are shown in Fig. 13(b). By comparing Fig. 13(a) and Fig. 13(b), it can be seen that the clock skew estimates converge to their expected values after 5K samples (or after 1.8\(\mu\)s). Note that the convergence time depends on the simulated parameters such as input frequency, number of channels, and channel mismatches. To analyze the key differences between the proposed calibration and the state of the art, Table I presents the reported available convergence time and main characteristics of the prior art techniques.

**TABLE I: Comparison with the state of the art techniques.**

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<tbody>
<tr>
<td>Background</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Blind</td>
<td>Yes</td>
<td>Yes</td>
<td>semi-blind</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Input in any NB</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Add ref. channel</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Pilot input injection</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>(M) (# of Channels)</td>
<td>12</td>
<td>4</td>
<td>2</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Clock freq. of filter</td>
<td>(f_s)</td>
<td>(f_s)</td>
<td>(f_s)</td>
<td>(f_s/M)</td>
<td>(f_s/M)</td>
</tr>
<tr>
<td>Cal. Manner</td>
<td>FF</td>
<td>FB</td>
<td>FB</td>
<td>FF</td>
<td>FF</td>
</tr>
<tr>
<td>Conv. time</td>
<td>10K</td>
<td>1.5K</td>
<td>4K</td>
<td>10K</td>
<td>5K</td>
</tr>
</tbody>
</table>

Fig. 14 illustrates SNDR and SFDR versus the baseband frequencies to which the subsampling TIADC folds the input frequency at higher NB back. As can be seen, the SNDR and SFDR before calibration decrease with the input frequency and the NZ order increment. This is because the impact of timing skew increases with input frequency [3]. After calibration, the SFDR remains smaller for higher NZs. This is due to the fact that (i) (8) and (2) are obtained by employing the Taylor series to the first derivative once assuming the sample-time error small; (ii) the derivative signals in (2) and (19) are computed using the incorrected sub-ADC outputs instead of input. These approximations become less accurate as the distortion level rises. Nevertheless, the proposed technique achieves the SFDR improvement of at least 28dB and 60dB SNDR over the first four NBs, which proves the efficiency and added value of the proposed technique.

Fig. 15 shows the SNDR and SFDR versus the standard deviation \(\delta_{te}\) of clock skews for the input at frequency \(f_{IN} = 0.45f_s + \frac{f_s}{2}\) in the second NZ. The solid and dash-dot curves show the performance after and before calibration, respectively. SNDR and SFDR before calibration decrease when timing skews increases. This is because the impact of timing mismatch rises with clock skews. The proposed calibration significantly improves the linearity up to 97dB SFDR for \(\delta_{te}\) less than 0.2\(\mu\)s.

The presented feedforward calibration is also validated for a band-limited bandpass multitone input signal. Fig. 16 shows the output spectrum with/without calibration for a 47 sinusoidal tone input in the second NB with \(f_L = 0.05f_s + \frac{f_s}{2}\), and \(f_H = 0.45f_s + \frac{f_s}{2}\). As illustrated in Fig. 16, undersampling TIADC directly down-converts the bandpass input to the frequency baseband \((0, \frac{f_s}{2})\), i.e., \(f_H\) and \(f_L\) map to 0.1\(f_s\) and 0.45\(f_s\) due to the second NZ sub-sampling, respectively. It can be seen that spurs due to timing skews are reduced to the noise floor. The proposed technique obtains the SNDR improvement of approximately 14dB.

**B. Hardware Implementation and Validation**

FPGA and ASIC design flow using Matlab/Simulink in [19], [24], [26] is applied in this framework. The hardware architecture of the proposed calibration is designed and optimized in term of fixed-point representation of signals that is characterized by signal ranges and signal Word-Length (WL). In the Optimal Fixed-point Simulink (OFpS) model, its parameters need to be optimized, i.e. the order of FIR filters and the signal WLs. The signal ranges of block signals in the OFpS model are mathematically computed based the transfer function of DSP blocks and simulations as done in [24]. The signal ranges
would determine the fractional factors used to convert signal values into binary representation meanwhile the WLs impact on SNDR/SFDR performance. Thus, the optimal FIR orders and the WLs of all block signals are optimized based on SNDR/SFDR metrics as presented in Fig. 11 for an example of the FIR order optimization and in Fig. 17 for the corrected sub-ADC outputs. As can be seen in Fig. 17, the number of bits is assigned to the compensated sub-ADC outputs is 14 bits.

The OFpS model (or hardware architecture) processes real-time signal data in sample-by-sample manner. Therefore, the delays of each signal datapath are made balanced. Note that, pipeline registers are inserted to reduce the combinational path length and improve the global working frequency and throughput [19]. Fig. 18 shows the pipelined OFpS architecture of the proposed calibration for four-channel TIADCs.
the FPGA and dissipates few percentages of the hardware resources of FPGA chip.

1) ASIC synthesis: The ASIC design flow proposed in [19], [26] is applied in this framework. The HDL design is synthesized to a gate-level netlist using Cadence RTL Compiler (RC) targeting the ST-28nm FD-SOI technology. The RC synthesis tool uses the automatic datapath retiming techniques in order to improve the working frequency. To make more efficient power savings, automatically inserting clock-gating logic for register banks is executed by the low power (RC-LP) engine. The RC-LP engine identifies when the registers are inactive and disables the clock during these periods. Once timing requirements are fulfilled, automatic placement and routing are performed using Cadence Encounter Place and Route (P&R) tool. During the P&R phase, clock tree synthesis is also performed and the clock buffers are placed to ensure correct clock propagation and synchronization in the design [19]. The P&R logic simulations is performed using the P&R Verilog gate-level netlist and the Verilog testbench generated by Matlab HDL coder Toolbox. Verilog Value-Change Dump (VCD) file generated by P&R logic simulations contains the information about value changes on selected signals. Reading switching activity information from a VCD file by Encounter RTL compiler provides the detailed information about the switching behavior of nets and ports, which leads to more accurate power estimation [19].

Note that the fixed point coding, optimization of the filter coefficients and the signal path Word-Length (WL) were performed using Matlab-Simulink. Using this study, the Verilog code was created and thus the output of the modelsim simulation is to be identical to the output of the Matlab simulink simulations as long as there are no timing errors in the modelsim simulations. Thus, if there is no error after the post P&R logic simulations, the achieved output of the synthesized circuit after the layout simulations is the same as the output of the fixed-point simulink model.

Using the polyphase implementation, the working clock frequency of the synthesized circuit is $f = 675$ MHz. The post P&R logic simulations are executed without any error messages at 2.7GHz, i.e., reporting that Total Negative Slack (TNS = 0), Worst Negative Slack (WNS = 0.78ns), and no violating paths. The overall speed of the calibration system is 2.7GHz. It consumes a total power of 33.2mW at input frequency 5.3GHz in the fourth NZ and occupies the 0.04mm² area. The synthesized calibration system uses 26032 logic gates in total as shown in Table II.

![Fig. 19(a) Power pie chart and (b) Module locality of the chip die area](image)

The above calibration system design works properly for the sub-sampling ADC with the input up to NZ4. Considering the baseband (or Nyquist) ADC applications, the calibration is dedicated to design for the input in the first NB. In this case, the digital background calibration unit dissipates 15.5mW total power at input frequency 1.2GHz in the first NZ and occupies the 0.02mm² chip area. 11214 logic gates are used in the digital unit as presented in Table III. The power dissipation of the digital calibration unit for the baseband ADC is 50% lower than the circuits dedicated for sub-sampling ADCs. Actually, for this latter, we have a higher signal WLs and the addition of FIR Hilbert filter, NZ order dependent scale factor to the Nyquist derivative filter.

2) Measurement Set-up: This section is dedicated to the results achieved by post processing the measured data using the TIADC board provided by NXP semiconductor and published in [6]. The chip is a 64-channel 11-b time-interleaved SAR ADC clocked at 2.7GHz. 64 channels are divided into 4 quarters. Each quarter consists of the interleaved 16 SAR ADCs which share the same sample and hold. The effect of timing mismatch in this TIADC is therefore equivalent to the timing mismatch in four-channel TIADCs. This is the reason why the above simulations were carried for the four-channel TIADC in order to demonstrate the efficiency of our solution. Note that offset and gain mismatches are static and frequency independent. Their impacts are the same for both subsampling and regular baseband TIADCs [19], [27]. Moreover, the offset

<table>
<thead>
<tr>
<th>Type</th>
<th>Instances</th>
<th>Area [$\mu$m²]</th>
<th>Area %</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sequential</td>
<td>4185</td>
<td>18367.181</td>
<td>41.6</td>
</tr>
<tr>
<td>Inverter</td>
<td>5905</td>
<td>1963.459</td>
<td>4.4</td>
</tr>
<tr>
<td>Buffer</td>
<td>449</td>
<td>240.067</td>
<td>0.5</td>
</tr>
<tr>
<td>Logic</td>
<td>15493</td>
<td>23600.106</td>
<td>53.4</td>
</tr>
<tr>
<td>Total</td>
<td>26032</td>
<td>44170.813</td>
<td>100.0</td>
</tr>
</tbody>
</table>

the DPF block dissipates 45% of the total power significantly more power than the other sub-modules. Fig. 19(b) displays the physical locality of the sub-modules on the chip of the synthesized and designed digital circuit. The DPF block formed from the digital polyphase filter components of BD FIR filter occupies the biggest part of the chip die area.
and gain calibrations integrated on the ADC chip can be turned on/off by software. Thus, all-digital offset and gain mismatch calibrations are proposed in this framework in order to tackle all channel mismatches in subsampling TIADCs with the real samples captured from the chip.

A simple way of canceling the offset error is to calculate the modified moving average of each sub-ADC output and then subtract the average results from their respective sub-ADC outputs samples [27]. The offset-corrected samples are then passed into the gain mismatch calibration unit where gain mismatch is mitigated. The relative gain of each sub-ADC with respect to a reference sub-ADC is determined by computing a power ratio between the average powers of sub-ADCs and reference channel. The relative gain estimate is multiplied with the according sub-ADC output samples to generate the corrected sub-ADC output [26]. The gain-corrected channels have the same gain values of the reference channel, hence equalizing gain mismatch among ADC channels.

The offset and gain corrected samples are then transmitted to the pipelined OFpS architecture where clock skews are corrected by our proposed calibration. The pipelined OFpS model is in fact equivalent to the synthesized digital circuit as interpreted in section IV-B1. Thus, the emulated results also present the efficiency of our solution when it is integrated on the ADC chip.

The measurement set-up used to measure the TIADC output, is described in Fig. 20. The various equipments are set up as follows:

• Arbitrary signal generators up to 6GHz.
• A 2.7GHz external clock generator needs to supply the clock signal to the ADC chip. The input signal generators and the clock signal generator are synchronized through a reference signal (10MHz).
• Narrow band filters are used for the input signal frequency to remove the harmonics (or distortions) created by the input signal generators and achieve a pure sine-wave at the input of the ADC.
• Because of the limited Random-Access Memory (RAM) (limited to 16K samples) of the ADC chip, the TIADC is connected to a FPGA DE4 board via a SATA connection. The SATA interface is made of the two differential links connected to the FPGA board. Because of the limited speed of the SATA bus, the ADC output is downsampled by 5. The downsampled output sequence is saved in the FPGA RAM that can store up to $2^{18} = 262144$ samples. This determines the resolution of the power spectral density (PSD).
• Measured data is transferred to a Personal Computer (PC) via an I2C connection for post processing calibrations.

For the measurement, the offset and gain calibrations embedded on the chip are turned off. Two-tone sinusoidal input is created at frequency $f_{in} = [2300MHz, 2301MHz]$ in the second NB. The same powers of the two tones are equal to $-1dBm$. The frequency gap between the two tone is 1MHz. This is because the generated input is guaranteed inside the bandwidth of a narrow band filter.

Fig. 21(a) and (b) show the output spectrum before and after executing the proposed all-digital offset and gain calibrations. respectively. The output of the ADC chip is distorted by channel mismatches (offset, gain and clock skew) and non-linear harmonic distortion coming from the electrical components of the ADC front-end. Note that due to sub-sampling and downsampling processes, input tones map to 140MHz and 141MHz, respectively as shown in Fig. 21. Obviously, the offset tones are completely removed out after calibration. The spurs due to timing skew and gain mismatches have the same position at the output spectrum [3]. As can be seen, the gain calibration compensates the real samples and reduces.

Fig. 21: Measured output spectrum after and before calibration (due to sub-sampling and downsampling two original input tones map to 140MHz and 141MHz, respectively)
the level of some spurious tones (not all) induced by clock skews and gain mismatches by around 3dB. The corrected output samples by offset and gain calibration are fed into the optimal hardware architecture illustrated in Fig. 18 to mitigate the clock skew errors. Fig. 21(c) illustrates the output spectrum after performing the proposed calibration algorithm. As can be seen, the proposed clock skew calibration significantly mitigate the skew and gain spur levels to the noise floor level from $-66$dBFS to $-97$dBFS. During calibration, the timing mismatch coefficients converge to their expected values after 5K samples (or $1.8\mu s$) as shown in Fig. 22. From the above measurement results, the ADC chip suffers from nonlinear distortions coming from the front-end of the ADC. The effects of these distortion errors can be removed out by applying the digital distortion compensation techniques presented in [39], [40].

By making a survey of the TIADC chips published at the ISSCC and VLSI conferences from 1997 to 2016 [41], if the clock skew calibration is needed, most TIADC chip used the mixed-signal calibration. Table IV shows the performance comparison of the synthesized digital logic of only clock skew calibrations to the state-of-the-art techniques. The designed digital logic of the proposed calibration system successfully tackles the timing skew problem for input at any NB. In post-processing simulations with the real data captured from the ADC chip, it keeps skew tones at $-97$dBFS for two-tone sinusoidal input located in the second NZ at frequencies of $2300$MHz, $2301$MHz. Moreover, it dissipates less power and work at higher sampling rate than the prior arts. With $31$dB improvement of clock skew induced spur levels, the proposed calibration has the same emulation performance as our previous work reported in [19], [26]. However, it consumes $7.5$mW less power after post P&R logic simulations than our previous one in [19], [26], i.e., reducing 19% power consumption. This is because the proposed calibration saves one more BD filter in design. Furthermore, with $15.5$mW power consumption and $0.02$mm$^2$ chip area of the synthesized calibration circuit for the baseband ADCs clocked at $2.7$GHz presented in Section IV-B1, our solution outperforms the state-of-the-art in terms of low power consumption and high sampling rate.

![Fig. 22: Convergence speed of clock skews with post-processing the real samples.](image)

### TABLE IV: Performance Comparison

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<tr>
<td>$M$</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Rate (GS/s)</td>
<td>2.7</td>
<td>2.7</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Resolution</td>
<td>11 bits</td>
<td>11 bits</td>
<td>10 bits</td>
<td>12 bits</td>
</tr>
<tr>
<td>Input</td>
<td>Up to NZ4</td>
<td>Up to NZ4</td>
<td>NZ1</td>
<td>NZ1</td>
</tr>
<tr>
<td>Spurs (dBFS)</td>
<td>$97@f_{in}$</td>
<td>$97@f_{in}$</td>
<td>$90.3 @ 0.99$MHz</td>
<td>$70 @ 750$MHz</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>33.2</td>
<td>41</td>
<td>171</td>
<td>35.3</td>
</tr>
</tbody>
</table>

$1f_{in} = \{2300$MHz, $2301$MHz$\}$

digital logic of the proposed calibration system successfully tackles the timing skew problem for input at any NB. In post-processing simulations with the real data captured from the ADC chip, it keeps skew tones at $-97$dBFS for two-tone sinusoidal input located in the second NZ at frequencies of $2300$MHz, $2301$MHz. Moreover, it dissipates less power and work at higher sampling rate than the prior arts. With $31$dB improvement of clock skew induced spur levels, the proposed calibration has the same emulation performance as our previous work reported in [19], [26]. However, it consumes $7.5$mW less power after post P&R logic simulations than our previous one in [19], [26], i.e., reducing 19% power consumption. This is because the proposed calibration saves one more BD filter in design. Furthermore, with $15.5$mW power consumption and $0.02$mm$^2$ chip area of the synthesized calibration circuit for the baseband ADCs clocked at $2.7$GHz presented in Section IV-B1, our solution outperforms the state-of-the-art in terms of low power consumption and high sampling rate.

### V. CONCLUSION

This framework has presented an all-digital clock skew feedforward background calibration for sub-sampling TIADCs. This technique does not require a pilot input nor additional reference channel. It is implemented using the polyphase filtering technique in order to enhance the working frequency in the DSP and does not use adaptive filter banks which enable the implementation at a moderate hardware and also improve the power consumption. Moreover, the correction and estimation algorithms in the feedforward calibration scheme re-use (or share) the common BD FIR filter which is able to save filter hardware and reduce 19% power dissipation. Simulations demonstrate the efficiency of the proposed calibration which leads to SFDR improvement of at least $28$dB over the first four NZs. The pipelined hardware architecture of the proposed calibration is optimized using the fixed-point optimization methodology. The HDL design of the pipelined hardware architecture has been synthesized using RC targeting ST-28nm FD-SO1 process. The designed digital circuit successfully addresses the clock skew problem for the 60x1B SNR sub-sampling and baseband TIADC applications clocked at $2.7$GHz. For undersampling TIADC applications, it occupies an area of $0.04$mm$^2$ and dissipates a total power of $33.2$mW at the input frequency of $5.3$GHz; and it has $0.02$mm$^2$ area occupation and $15.5$mW power consumption at the input frequency of $1.2$GHz for baseband ADC applications. In comparison with the state-of-the-art, our solution achieves small chip area, lower power consumption and higher rate. By post processing the measured data from the ADC chip, the clock skew calibration combines with the classical calibration algorithms of gain and offset mismatches to successfully address all channel mismatches. The clock calibration keeps the timing mismatch tones below $-97$dBFS for the two-tone sinusoidal input in the second Nyquist Zone in post processing the measured data stream from the ADC chip, demonstrating the outperforming of our solution compared with prior arts.

### ACKNOWLEDGMENT

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### REFERENCES


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At UC Berkeley, he has proposed “COGNICOM”, a brain-inspired software-hardware paradigm, to support IoT’s future growth. COGNICOM brings computing closer to end-user and focuses on optimal uses of local Smart Application Gateway and cloud computing. COGNICOM consists of two key components: Cognitive Engine and Smart Connectivity. The cognitive engine is powered by deep-learning algorithms integrated with game-theoretic decision analytics, implemented on low-power Network Multi-Processor System on Chip. The cognitive engine provides cognitive functions (e.g. anomaly detection and decision making) to smart objects. SC integrates neural network inspired designs of cognitive radio, transceivers and baseband processors. The smart connectivity provides flexible and reliable connections to IoT objects and optimally distributes communication resources. The designs of both cognitive engine and smart connectivity will leverage his past success in designing cognitive radios and surveillance game.

He moved to Stanford University on July 1st 2016.