Operational Semantics of Ada Ravenscar

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Abstract. The Ada programming language has been designed from the ground up for safety-critical real-time systems. This trend has continued with the Ada 2005 language definition which has incorporated the Ravenscar Profile for high-integrity systems into the language standard. Here we describe the operational semantics for Ada Ravenscar code generated automatically from an architecture description of the system given in the Architecture Analysis and Design Language.

1 Introduction

The Ada Ravenscar Profile [2] is a restriction of the rich tasking subset of the Ada language and associated runtime that aims to make the language more amenable to the development of safety-critical real-time systems. The Architecture Analysis and Design Language (AADL) [13] is an architecture description language targeted specifically to the real-time and avionics domain. The code generation rules given with the AADL standard are incomplete and rely on the existance of an "AADL executive", in effect, an operating system that provides all the services needed by an AADL application.

Since such an operating system does not exist, we used ORK [6], a Ravenscarcompliant executive. We developed code generation rules for AADL to Ada that faithfully preserve semantics when run on the ORK platform. We also developed a code generator as an Eclipse plugin (ARC http://aadl.enst.fr/arc/) that transforms AADL models to Ada source. The code generation rules and toolset were introduced in [9]. In this paper, we present a static semantics for the Ravenscar code that we generate, which is a subset of Ada Ravenscar. We also present a structured operational semantics that represents the dynamic evolution of the generated system. The Ravenscar Profile restrictions on Ada eliminate certain features from the language and associated runtime:

- All tasks must be either periodic or sporadic (for schedulability analysis)
- Tasks may only communicate among themselves through protected objects
- No dynamic creation or destruction of tasks or protected objects
- Rendezvous are prohibited (no entries on Ada tasks)
- Protected objects may have at most one entry
- A protected object entry's queue is of size 1
- All delays must be absolute (no delay <time_expression> allowed)

- Scheduling is priority based, priority assignment is RMA [15] or RTA [3]
- The priority ceiling protocol [16] is used for access to protected objects

ARC relies upon the OSATE AADL toolkit [14] to parse AADL models. The OSATE toolkit uses the Eclipse Modeling Framework [1] to represent the abstract syntax of the parsed model. Instead of directly generating Ada code from the AADL model, we chose to implement an intermediate meta-model to represent the Ravenscar system. The front-end transforms the AADL model to an instance of this meta-model. The code generator traverses this intermediate model—which we call the Ravenscar Meta-model (RMM)—to generate Ada code. Two advantages of this approach are a reduction in complexity (RMM is simpler than the AADL meta-model), and ease of writing code generators for other languages. Because all AADL models cannot be transformed to Ravenscarcompliant code, we verify the AADL model against a set of Object Constraint Language rules before a model transformation from AADL to an instance of the RMM is carried out. The paper is structured as follows. Sec. 2 presents the static semantics. Sec. 3 presents the dynamic semantics of the generated Ravenscar code using a structured operational semantic approach [12]. Sec. 4 relates our contribution to past and ongoing research and concludes.

2 Static Semantics

The static semantics provided in this section are a formalization of the structure of the RMM using set theory, and mirrors the static structure of code generated by ARC. This static semantics will be used in the ensuing section on dynamic semantics, specifically to manipulate the entities in the operational semantic transitions.

2.1 Ravenscar Computational Units

A Ravenscar system is given by five *finite* and *pairwise disjoint* sets, endowed with five functions and related by four relations. The five sets are:

Periodic tasks $\mathcal{T}_p = \{P_1 \dots P_n\}$ Sporadic tasks $\mathcal{T}_s = \{S_1 \dots S_m\}$ Interrupts $\mathcal{U} = \{U_1 \dots U_k\}$ Synchronisers $\mathcal{D} = \{D_1 \dots D_l\}$ Exchangers $\mathcal{E} = \{E_1 \dots E_r\}$

- Sporadic tasks are dispatched upon the reception of an event. A minimum time—characteristic to each task—between successive dispatches is enforced
- Periodic tasks are dispatched at regular time intervals called their period
- Interrupts can be raised at any time except if a previous occurence is already being executed. Thus, at any time, there can be at most $k = |\mathcal{U}|$ interrupts present in the system

- Exchangers are protected objects with an internal data buffer and Get and Set procedures. They are used for simple data exchange among tasks
- Synchronisers are protected objects with an internal queue of events that expose a Send_Event procedure for depositing events. A Get_Event entry is exposed upon which the associated sporadic task waits for dispatch

We define four derived sets, namely, Tasks (\mathcal{T}) , Activities (\mathcal{A}) , Protected objects (\mathcal{PO}) , and Computational units (\mathcal{C}) ; as follows:

$$egin{aligned} \mathcal{T} &= \mathcal{T}_p \cup \mathcal{T}_s \ \mathcal{A} &= \mathcal{T}_p \cup \mathcal{T}_s \cup \mathcal{U} \ \mathcal{PO} &= \mathcal{E} \cup \mathcal{D} \ \mathcal{C} &= \mathcal{A} \cup \mathcal{PO} \end{aligned}$$

2.2 Functions on Computational Units

Five functions on computation units are defined with the following signatures:

- $PRIORITY: \mathcal{C} \to \text{Anypriority}$ (1)
- HOLDINGTIME: $\mathcal{T} \to \text{TIME}$ (2)
 - $PROG: \mathcal{C} \to \mathbb{PROGS}$ (3)

TIME is a discrete time domain. HOLDINGTIME is defined as the period for a periodic and minimum inter-dispatch time for a sporadic task. ANYPRIORITY is a bounded subset of the set \mathbb{N} of natural numbers and gives valid priorities. PROGS is the subset of Ada 95 that the code of computational units conforms to. The code of a computational unit γ is given by $PROG(\gamma)$.

2.3 Conformant PROGS Programs

We focus on an abstraction of programs that represents execution steps relevant to our semantics, which gives legal instructions and their sequencing:

- comp: A sequential execution step
- Set(E): A Set call to exchanger E
- Get(E): A Get call to exchanger E
- Send_Event(D): A Send_Event call to synchroniser D
- Get_Event(D): A Get_Event call to synchroniser D
- delay until: request to be suspended until a future instant
- ret: return statement

The legal execution sequences of these steps depend on the type of the computational unit. They are defined using BNF grammars. The code of each computational unit must respect its prescribed grammar (BP is for periodic tasks, BS for sporadic, BU for interrupts, BE for exchangers, BD for synchronizers): $\begin{array}{l} \operatorname{BP} := \operatorname{comp}; \operatorname{BP} \mid \operatorname{Set}(E); \operatorname{BP} \mid \operatorname{Get}(E); \operatorname{BP} \mid \operatorname{Send_Event}(D); \operatorname{BP} \mid \operatorname{delay} \text{ until} \\ \operatorname{BS} := \operatorname{Get_Event}(D); \operatorname{BP} \\ \operatorname{BU} := \operatorname{Send_Event}(D) \mid \operatorname{Set}(E) \\ \operatorname{BE} := [\operatorname{Send_Event} - > \operatorname{CC}, \operatorname{Get} - > \operatorname{CC}] \\ \operatorname{BD} := [\operatorname{Send_Event} - > \operatorname{CC}, \operatorname{Get_Event} - > \operatorname{CC}] \\ \operatorname{CC} := \operatorname{comp} ; \operatorname{CC} \mid \operatorname{ret} \end{array}$

2.4 Topological Relations on Computational Units

By an analysis of the set of programs PROG, we can construct the communication topology between the various computational units. Four topological relations, *sets, gets, sends_event*, and *gets_event* are induced by PROG:

$$sets: \underbrace{}_{\mathsf{Set}} \subset \mathcal{A} \times \mathcal{E} \tag{4}$$

$$gets: -\frac{1}{\operatorname{Get}} \subset \mathcal{T} \times \mathcal{E}$$

$$\tag{5}$$

$$sends_event: _ \bigcirc \mathcal{A} \times \mathcal{D}$$
(6)

they are defined according to the following conditions:

$$\operatorname{Set}(E) \text{ occurs-in } \operatorname{PROG}(\alpha) \quad \Leftrightarrow \quad \alpha \underbrace{\operatorname{Set}}_{E} \tag{8}$$

$$Get(E)$$
 occurs-in $PROG(T)$ \Leftrightarrow $T - \frac{1}{Get} E$ (9)

$$Send_Event(D) \text{ occurs-in } PROG(\alpha) \quad \Leftrightarrow \quad \alpha - \frac{D}{Send_Event} D \quad (10)$$

$$Get_Event(D) \text{ occurs-in } PROG(S) \quad \Leftrightarrow \quad S \xrightarrow{} D \quad (11)$$

We also need three derived relations, namely: dispatches $(__{DTS}]$, writes_to $(__{WTO}]$ and accesses $(__{ACC}]$. dispatches is the inverse of gets_event, writes_to is the union of gets and sends_event, and accesses is the union of the four primitive relations. Formally:

$$D_{-DIS} S \triangleq S_{-\text{Get_Event}} D \tag{12}$$

$$\alpha \xrightarrow{WTO} \pi \triangleq (\pi \in \mathcal{E} \land \alpha \xrightarrow{\mathsf{Set}} \pi) \lor (\pi \in \mathcal{D} \land \alpha \xrightarrow{\mathsf{Send_Event}} \pi)$$
(13)

$$\alpha \xrightarrow{ACC} \pi \triangleq (\pi \in \mathcal{E} \land \alpha \xrightarrow{\text{Set}} \pi) \lor (\pi \in \mathcal{E} \land \alpha \xrightarrow{\text{Get}} \pi)$$
(14)
$$\lor (\alpha \in \mathcal{A} \land \pi \in \mathcal{D} \land \alpha \xrightarrow{\text{Send_Event}} \pi)$$
$$\lor (\alpha \in \mathcal{T}_s \land \pi \in \mathcal{D} \land \alpha \xrightarrow{\text{Get_Event}} \pi)$$

The topological relations must satisfy the following constraints:

$$\forall D, \exists S \text{ unique satisfying: } D_{\overline{DIS}} S \tag{15}$$

$$\forall S, \exists D \text{ unique satisfying: } S \underbrace{}_{\text{Get Event}} D \tag{16}$$

$$\forall U, \exists \pi \text{ unique satisfying: } U \xrightarrow[WTO]{WTO} \pi$$
(17)

$$U \xrightarrow{WTO} \pi$$
 and $U' \xrightarrow{WTO} \pi \Rightarrow U = U'$ (18)

At most one task is dispatched by a synchronizer (15). For every sporadic task, there exists one and only one synchronizer that dispatches it (16). Each interrupt writes on one and only one protected object (17). At most one interrupt may write to a protected object (18). Constraints (15) and (16) imply that relations $\frac{DIS}{DIS}$ and $\frac{\text{Get.Event}}{\text{Get.Event}}$ are bijective and mutually inverse functions. From (17) and (18) it follows that relation $\frac{WTO}{WTO}$, when restricted to \mathcal{U} , is an injective function with co-domain in \mathcal{PO} .

Priority Ceiling Protocol. All priorities must comply with PCP. Function PRIORITY must satisfy the following property ($\frac{1}{ACC}$ from equation 14):

For any activity
$$\alpha$$
 and any protected object π :
 $\left(\alpha \xrightarrow[ACC]{} \pi\right) \Rightarrow \text{PRIORITY}(\pi) \geq \text{PRIORITY}(\alpha)$
(19)

3 Dynamic Semantics

The dynamic semantics of the system will be described using a form of *structured* operational semantics [12] which describes the evolution of the system over time.

3.1 Execution Context

Execution context
$$c = \begin{cases} \sigma, \sigma_s \text{ Scheduler} \\ \iota \text{ Idle task} \\ a \text{ An active execution context} \end{cases}$$

The above equation states that three entities may possess processing resources, the scheduler (σ and σ_s), the system idle task (ι), or an activity (a). The scheduler can be in one of two states: σ when the scheduler has seized control, σ_s when the scheduler is ready to grant control. Thus, σ and σ_s represent two steps in the excuction of the scheduler functions, allowing the assignment of different execution times to both in order to accurately model context switches. An active context, a, may have one of the following forms:

The PRIORITY function is extended to active contexts and in conformance with the priority ceiling protocol, as follows (where the form $\alpha - \frac{1}{x}\pi$ corresponds to the context of a protected object π executing a call x issued by activity α):

$$\operatorname{PRIORITY}(\alpha - \pi) = \operatorname{PRIORITY}(\pi)$$
(20)

We use a record notation—as defined in [4]—to maintain the state information of computational units. The fields corresponding to each computational unit are given in Table 1. We will use the dot notation to extract fields from records. $T \cdot Beh$ is the value of field Beh in the record T. The update of a field in a record is performed as in the following example where D' is the record obtained by updating in record D the field Bar with true and field Queue with ϵ :

$$D' = \langle D \leftarrow \mathsf{Bar} = \mathsf{true} \leftarrow \mathsf{Queue} = \epsilon \rangle$$

Description of field	Name	Type	\mathcal{D}	Е	\mathcal{T}_{s}	\mathcal{T}_p	\mathcal{U}
Current program state	Beh	PROGS					
Next dispatching time	Nd	TIME			\checkmark		
Elapsed time	Et	TIME			\checkmark	\checkmark	
Processing time	Pt	TIME					
Queue on entry	Queue	$\mathcal{T}_s \cup \{\epsilon\}$					
Barrier state	Bar	BOOL					
Event count	Ec	\mathbb{N}					

Table 1. Fields present in state records of Ravenscar Computational Units

3.2 Ready Queue

A ready queue, R, is made of a (possibly empty) sequence of active execution contexts. We use \circ as a sequence operator, hence, if a is an execution context and R a ready queue then $(a \circ R)$ is a ready queue whose head is a and whose tail is R. The empty ready queue will be denoted by ϵ . Ready queues satisfy the *priority-ordered* property, which is inductively defined as follows:

(i)
$$\epsilon$$
 is priority-ordered
(ii) $a \circ R$ is priority-ordered iff: $-R$ is priority-ordered and
 $-\forall a' \in R$: PRIORITY $(a') \leq$ PRIORITY (a)

The satisfaction by a queue R of the *priority-ordered* property implies that R is an ordered list of queues having the form: $R = r_{p_1} \circ \ldots \circ r_{p_n}$ where for each r_{p_n} :

$$\forall i, j : i < j \implies p_i > p_j \qquad \text{and} \tag{21}$$

$$\forall i, \ \forall a \in r_{p_i} : \text{PRIORITY}(a) = p_i \tag{22}$$

All active contexts in the same subqueue have the same priority (22), and subqueues are ordered according to their priorities (21). We define priority head insertion and priority tail insertion for ready queues as both methods are used: Let $p_k = \text{PRIORITY}(a)$ Priority Head Insertion $a \odot R =$

 $\begin{array}{l} r_{p_1} \circ \ldots \circ a \circ r_{p_k} \circ \ldots \circ r_{p_n} \text{ when } R = r_{p_1} \circ \ldots \circ r_{p_k} \circ \ldots \circ r_{p_n} \\ r_{p_1} \circ \ldots \circ r_{p_i} \circ a \circ r_{p_j} \ldots r_{p_n} \text{ when } R = r_{p_1} \circ \ldots \circ r_{p_i} \circ r_{p_j} \circ \ldots \circ r_{p_n} \wedge p_i < p_k < p_j \end{array}$

Priority Tail Insertion $R_{\odot}a =$

 $r_{p_1} \circ \ldots \circ r_{p_k} \circ a \circ \ldots \circ r_{p_n} \quad \text{when} \quad R = r_{p_1} \circ \ldots \circ r_{p_k} \circ \ldots \circ r_{p_n}$ $r_{p_1} \circ \ldots \circ r_{p_i} \circ a \circ r_{p_j} \ldots r_{p_n} \quad \text{when} \quad R = r_{p_1} \circ \ldots \circ r_{p_i} \circ r_{p_j} \circ \ldots \circ r_{p_n} \land \quad p_i < p_k < p_j$ (24)

A task taken from the blocked set to the ready queue is inserted at the tail of the ready queue for its priority, whereas one that is preempted during execution by the scheduler is inserted at the head of the ready queue for its priority.

3.3 Structure of the State of a Ravenscar System

The state of a Ravenscar system has a static part made up of the set of records of all computational units, and a dynamic part which is given by the vector:

$$IL \rightsquigarrow [c, R, B, \mathsf{ns}, \mathsf{t}]$$
 (25)

(23)

- − *IL*: list of interrupts present in the system, waiting to be handled. When the list of interrupts is empty, the leading "*IL* \sim " may be ommitted
- -c: current execution context
- R: ready queue
- B: set of blocked tasks
- ns: time of the next system clock tick when control is passed to the scheduler
- t: current time, i.e.: the current age of the system

Each of the execution context types (scheduler, idle, or active) may perform specific execution steps. These steps cause the state of the system to evolve over time. The steps performed by the active context depend on the current state of the code of its activity, given by the Beh field of the state record of the activity. The steps performable by the scheduler are: (i) suspending activity a and taking control $(a \xrightarrow{as} \sigma)$; (ii) suspending idle task and taking control ($(\iota \xrightarrow{is} \sigma)$; (iii) self suspention to handle interrupts ($\sigma_s \xrightarrow{ss} \sigma$); (iv) handling an interrupt ($\sigma \xrightarrow{ih} \sigma$); (v) updating the ready queue ($\sigma \xrightarrow{ud} \sigma_s$); (vi) granting control to activity a ($\sigma_s \xrightarrow{sa} a$); (vii) granting control to idle task ($\sigma_s \xrightarrow{si} \iota$). The idle task performs one type of steps which is idling: ($\sigma_s \xrightarrow{idling} \iota$).

3.4 Initial State of a Ravenscar System

The initial state of a Ravenscar system is given by:

$$\left[\sigma, R_0, B_0, 0, 0\right] \tag{26}$$

where the initial ready queue, R_0 , is a *priority-ordered* list of all tasks: $R_0 = T_1 \circ \ldots \circ T_n$, and B_0 the initial set of blocked tasks is an empty set: $B_0 = \{\}$. Moreover, the initial state of each of the periodic tasks, the sporadic tasks, the synchronisers and the exchangers, is given by their associated records:

$$\begin{split} P &= \langle \ \mathsf{Beh} = \operatorname{PROG}(P), \mathsf{Nd} = 0, \mathsf{Et} = 0, \mathsf{Pt} = 0 \ \rangle \\ S &= \langle \ \mathsf{Beh} = \operatorname{PROG}(S), \mathsf{Nd} = 0, \mathsf{Et} = 0, \mathsf{Pt} = 0 \ \rangle \\ E &= \langle \ \mathsf{Beh} = \operatorname{PROG}(E) \ \rangle \\ D &= \langle \ \mathsf{Beh} = \operatorname{PROG}(D), \mathsf{Queue} = \epsilon, \mathsf{Ec} = 0, \mathsf{Bar} = \mathsf{false} \ \rangle \end{split}$$

3.5 State Transitions of a Ravenscar System

The execution of a Ravenscar system is given by the set of structured operational semantics rules, having the structure of a fraction:

Antecedents			CHODT NAME
$\mathit{IL} \leadsto \left[c, R, B, ns, t \right]$	\xrightarrow{act}	$\mathit{IL'} \rightsquigarrow \left[c', R, 'B', ns', t\right] \hat{+} \delta(\mathit{act})$	SHURI NAME

Antecedents (numerator) are conditions which need to hold for the Consequent (denominator) part to be applied. Antecedents depend on the current state of the system. Consequent part denotes the transition taken and the action—act performed. act represents the smallest possible uninterruptible instruction. It is an indivisible unit; interrupts will either be fired before or after such an instruction. Complex instructions like **delay until** are considered a sequence of simpler instructions with the final indivisible one actually having the intended impact. IL and IL' are optional, they represent the list of interrupts present before and after the transition. $\delta(act)$ is the time consumed by the transition, and $\hat{+} \delta(act)$ is the ageing operator. It is formally defined as follows:

$$[c, R, B, \mathsf{ns}, \mathsf{t}] \stackrel{\sim}{+} \delta = [c \stackrel{\sim}{+} \delta, R \stackrel{\sim}{+} \delta, B, \mathsf{ns}, \mathsf{t} + \delta]$$

where:

$$c \hat{+} \delta = \begin{cases} \sigma & \text{if } c = \sigma \\ \iota & \text{if } c = \iota \\ \langle \alpha \leftarrow \mathsf{Et} = \alpha \cdot \mathsf{Et} + \delta \leftarrow \mathsf{Pt} = \alpha \cdot \mathsf{Pt} + \delta \rangle & \text{if } c = \alpha \lor c = \alpha \frac{1}{x} \\ R \hat{+} \delta = \langle a_1 \leftarrow \mathsf{Et} = a_1.\mathsf{Et} + \delta \rangle_{\circ} \dots \langle a_n \leftarrow \mathsf{Et} = a_n.\mathsf{Et} + \delta \rangle \text{ for } R = a_1 \circ \dots \circ a_n \end{cases}$$

The above equations state that if the currently executing task is either the scheduler or the idle task then the ageing operator has no effect on it. However, if the excution context is an active one then the ageing operator adds the $\delta(action)$ amount of time to both the elapsed time (Et) and processing time (Pt) fields of the record of the activity. On the other hand, for all tasks in the ready queue R, the ageing operator only adds the $\delta(action)$ amount of time to the elapsed time (item) amount of time to the elapsed time field (they are not budgeted for this time). We now provide the transition rules, starting with the system idle task and ending with rules for interrupt handling.

Idling: Rule *IDLE* shows the idle task executing. The antecedent shows that the system can only idle if it hasn't reached the next scheduling instant ns. The *age* of the system advances by an amount $\delta(\text{idling})$.

$$\frac{\mathsf{t} < \mathsf{ns}}{\begin{bmatrix} \iota, R, B, \mathsf{ns}, \mathsf{t} \end{bmatrix} \xrightarrow{\text{idling}} \begin{bmatrix} \iota, R, B, \mathsf{ns}, \mathsf{t} \end{bmatrix} \hat{+} \delta(\text{idling})} IDLE$$

Pure Computation Steps: The *CMPT* and *CMPO* transitions represent sequential computations that have no side-effects on tasking or inter-task communication. *CMPT* denotes a task carrying out a sequential computation, *CMPO* denotes a protected object carrying out a sequential computation. The behavior (Beh) must in both cases have comp instruction at the head, the current time must be less than the next dispatching time for the scheduler.

 $\begin{array}{c|c} T \cdot \mathsf{Beh} = \mathsf{comp}; \mathsf{C} & \wedge & \mathsf{t} < \mathsf{ns} \\ \hline \begin{bmatrix} T, R, B, \mathsf{ns}, \mathsf{t} \end{bmatrix} & \xrightarrow{\mathsf{comp}} & \begin{bmatrix} T', R, B, \mathsf{ns}, \mathsf{t} \end{bmatrix} \hat{+} \delta(\mathsf{comp}) \end{array} \quad CMPT \\ T' = \langle T \leftarrow \mathsf{Beh} = \mathsf{C} \rangle \end{array}$

$$\begin{array}{c} \pi \cdot \mathsf{Beh} = \mathsf{comp}; \mathsf{C} \quad \land \quad \mathsf{t} < \mathsf{ns} \\ \hline \left[\alpha \xrightarrow{x} \pi, R, B, \mathsf{ns}, \mathsf{t} \right] \xrightarrow{\mathsf{comp}} & \left[\alpha \xrightarrow{x} \pi', R, B, \mathsf{ns}, \mathsf{t} \right] \stackrel{?}{+} \delta(\mathsf{comp}) \end{array} \end{array} \mathcal{C}MPO \\ \pi' = \langle \pi \leftarrow \mathsf{Beh} = \mathsf{C} \rangle \end{array}$$

Protected Objects: The rule *NBCL* represents an activity (task or interrupt) calling a procedure of a protected object. The antecedent states that the current behaviour of the activity is a call to a procedure, and that the current time is less than the next scheduler launching time. The consequent is that the code of the protected object is being executed in the context of the activity α ($\alpha' = \pi$).

$$\begin{array}{ll} \alpha \cdot \mathsf{Beh} = x(\pi); C & \wedge \\ \hline x \in \{ \mathrm{Get}, \, \mathrm{Set}, \, \mathrm{Send_Event} \} & \wedge & \mathsf{t} < \mathsf{ns} \\ \hline \left[\alpha, R, B, \mathsf{ns}, \mathsf{t} \right] & \xrightarrow{x} & \left[\alpha' \xrightarrow{x} \pi, R, B, \mathsf{ns}, \mathsf{t} \right] \hat{+} \delta(x) \end{array} & NBCL \\ \alpha' = \langle \alpha \leftarrow \mathsf{Beh} = C \rangle \\ \pi' = \langle \pi \leftarrow \mathsf{Beh} = \mathrm{PROG}(\pi) . x \rangle \end{array}$$

The transitions RET1 through RET4 depict how calls from protected objects return. RET1 represents the return from a protected object procedure. The consequent shows that the execution time is budgeted to the task's processing time Pt. The calling activity is placed at the head of the ready queue and the scheduler takes control to evaluate barriers. RET2 shows a synchronizer returning from a Send_Event procedure when the entry queue is empty. Transition RET3 shows a synchronizer returning from a Send_Event procedure when

the entry queue is *not* empty. The blocked **Get_Event** entry is immediately executed in the context of the task waiting on it. *RET4* gives the situation where a synchronizer returns from **Get_Event** entry call. The task in whose context the execution was taking place is preempted and is placed at the head of its ready queue, and the scheduler takes over.

$$\begin{array}{c|c} E \cdot \mathsf{Beh} = \mathsf{ret} & \land & x \in \{\mathsf{Get}, \mathsf{Set}\} & \land & \mathsf{t} < \mathsf{ns} \\ \hline \left[\alpha \xrightarrow{x} E, R, B, \mathsf{ns}, \mathsf{t} \right] & \xrightarrow{\mathsf{ret}} & \left[\sigma, \alpha' \circ R, B, \mathsf{ns}, \mathsf{t} \right] \stackrel{?}{+} \delta(\mathsf{ret}) \end{array} & RET1 \\ \alpha' = \langle \alpha \leftarrow \mathsf{Pt} = \alpha \cdot \mathsf{Pt} + \delta(\mathsf{ret}) \rangle \end{array}$$

$$\begin{array}{ll} D \cdot \mathsf{Beh} = \mathsf{ret} & \land & D \cdot \mathsf{Queue} = \epsilon & \land & \mathsf{t} < \mathsf{ns} \\ \hline \left[\alpha \underbrace{\mathsf{-}_{\mathtt{Send_Event}} D, R, B, \mathsf{ns}, \mathsf{t}}_{} \right] & \stackrel{\mathsf{ret}}{\longrightarrow} & \left[\sigma, \alpha' \circ R, B, \mathsf{ns}, \mathsf{t} \right] \stackrel{?}{+} \delta(\mathsf{ret}) \end{array} & RET2 \\ D' = \langle D \leftarrow \mathsf{Bar} = \mathsf{true} \leftarrow \mathsf{Ec} = D \cdot \mathsf{Ec} + 1 \rangle \\ \alpha' = \langle \alpha \leftarrow \mathsf{Pt} = \alpha' \cdot \mathsf{Pt} + \delta(\mathsf{ret}) \rangle \end{array}$$

$$\begin{array}{l} D \cdot \mathsf{Beh} = \mathsf{ret} \ \land \ D \cdot \mathsf{Queue} = S \ \land \ \mathsf{t} < \mathsf{ns} \\ \hline \left[\alpha \underbrace{\mathsf{Get_Event}}_{\mathsf{Get_Event}} D, R, B, \mathsf{ns}, \mathsf{t} \right] & \xrightarrow{\mathsf{ret}} & \left[S' \underbrace{\mathsf{Get_Event}}_{\mathsf{Get_Event}} D', \alpha' \circ R, B', \mathsf{ns}, \mathsf{t} \right] \stackrel{?}{+} \delta(\mathsf{ret}) \end{array} \right] \\ B' = B \setminus \{S\} \\ S' = \langle S \leftarrow \mathsf{Nd} = \mathsf{t} + \mathsf{HOLDINGTIME}(S) \rangle \\ D' = \langle D \leftarrow \mathsf{Bar} = \mathsf{true} \leftarrow \mathsf{Ec} = D \cdot \mathsf{Ec} + 1 \rangle \\ \alpha' = \langle \alpha \leftarrow \mathsf{Pt} = \alpha \cdot \mathsf{Pt} + \delta(\mathsf{ret}) \rangle \end{array}$$

$$\begin{array}{ccc} D \cdot \mathsf{Beh} = \mathtt{ret}; \ \mathsf{C} & \wedge & \mathtt{t} < \mathtt{ns} \\ \hline & & \left[S_{\underline{\mathsf{Get}_\mathsf{Event}}} D, R, B, \mathtt{ns}, \mathtt{t}\right] & \xrightarrow{\mathtt{ret}} & \left[\sigma, S' \odot R, B, \mathtt{ns}, \mathtt{t}\right] \hat{+} \ \delta(\mathtt{ret}) \\ \hline & D' = \langle D \leftarrow \mathsf{Bar} = (D \cdot \mathsf{Ec} > 1) \leftarrow \mathsf{Ec} = D \cdot \mathsf{Ec} - 1 \leftarrow \mathsf{Queue} = \epsilon \rangle \\ & S' = \langle S \leftarrow \mathsf{Pt} = S \cdot \mathsf{Pt} + \delta(\mathtt{ret}) \rangle \end{array}$$

Rules *OBCL* and *CBCL* represent a sporadic task issuing a **Get_Event** call. Rule *OBCL* represents when the barrier is open and the call is immediately executed. Rule *CBCL* represents when the barrier is closed, the call remains blocked on the entry until a **Set_Event** is issued by another task or interrupt.

$$\begin{array}{l} S \cdot \mathsf{Beh} = \mathsf{Get_Event}(D) \ ; \ \mathsf{C} \land D \cdot \mathsf{Bar} = \mathrm{True} \land \mathsf{t} < \mathsf{ns} \\ \hline \left[S, R, B, \mathsf{ns}, \mathsf{t} \right] & \xrightarrow{\mathrm{Get_Event}} & \left[S' \xrightarrow{\mathrm{Get_Event}} D', R, B, \mathsf{ns}, \mathsf{t} \right] \widehat{+} \delta(\mathsf{Get_Event}) \end{array} \quad OBCL$$
$$S' = \langle S \leftarrow \mathsf{Beh} = C \leftarrow \mathsf{Nd} = \mathsf{t} + \mathsf{HOLDINGTIME}(S) \rangle$$
$$D' = \langle D \leftarrow \mathsf{Beh} = \mathsf{PROG}(D) \cdot \mathsf{Get_Event} \rangle$$

 $\begin{array}{l} S \cdot \mathsf{Beh} = \mathtt{Get_Event}(D) \, ; \ \mathtt{C} \ \land D \cdot \mathtt{Bar} = \mathtt{False} \ \land \ \mathtt{t} < \mathtt{ns} \\ \hline \begin{bmatrix} S, R, B, \mathtt{ns}, \mathtt{t} \end{bmatrix} & \xrightarrow{\mathtt{Get_Event}} & \begin{bmatrix} S', R, B, \mathtt{ns}, \mathtt{t} \end{bmatrix} \hat{+} \ \delta(\mathtt{Get_Event}) \end{array} \quad CBCL$ $\begin{array}{l} S' = \langle S \leftarrow \mathtt{Beh} = C \leftarrow \mathtt{Bar} = \mathtt{true} \rangle \\ D' = \langle D \leftarrow \mathtt{Queue} = S \rangle \end{array}$

Scheduler. The scheduler also takes control at certain points called *scheduling* points. Some of these have already been explained (the RET_i transitions). Others occur when the active context executes a delay until instruction, and when the scheduler is *scheduled* to execute, represented by the ns variable in the system configuration and calculated just before the scheduler cedes control. NS-IDLE and NS-ACT represent the scheduler preempting the idle task and an activity (respectively) as its launch time arrives. SDELAY and PDELAY show a sporadic task and a periodic task (respectively) execute a delay until. ns is the minimum of Nd fields of all tasks in the blocked set where Nd represents the next dispatching time for the task: $ns = \min_{T_i \in B}(T_i \cdot Nd)$. SCUD is the evolution of the scheduler as it evaluates and updates the ready queue and blocked tasks. SCAC shows the scheduler calculating its next dispatching time and then granting control to the highest priority ready task. SCID is the action carried out by the scheduler when the ready queue is empty.

$$\frac{\mathsf{ns} \leq \mathsf{t}}{\begin{bmatrix}\iota, R, B, \mathsf{ns}, \mathsf{t}\end{bmatrix} \xrightarrow{\mathrm{is}} [\sigma, R, B, \mathsf{ns}, \mathsf{t}] \stackrel{}{+} \delta(\mathrm{is})} NS\text{-IDLE}$$

$$\begin{array}{c} \mathsf{ns} \leq \mathsf{t} \\ \hline \hline \begin{bmatrix} a, R, B, \mathsf{ns}, \mathsf{t} \end{bmatrix} & \xrightarrow{\mathrm{as}} & \begin{bmatrix} \sigma, a \circ R, B, \mathsf{ns}, \mathsf{t} \end{bmatrix} + \delta(\mathrm{as}) \end{array} \quad \textit{NS-ACT} \end{array}$$

 $\begin{array}{c} T \cdot \mathsf{Beh} = \mathtt{delay}; \mathtt{C} \land \mathtt{t} < \mathtt{ns} \\ \hline \left[T, R, B, \mathtt{ns}, \mathtt{t}\right] \xrightarrow{\mathrm{delay}} \left[\sigma, R, B', \mathtt{ns}, \mathtt{t}\right] \hat{+} \delta(\mathtt{delay}) \\ T' = \langle T \leftarrow \mathtt{Beh} = \mathtt{PROG}(T) \leftarrow \mathtt{Pt} = T \cdot \mathtt{Pt} + \delta(\mathtt{delay}) \rangle \\ B' = B \cup \{T'\} \end{array}$

$$\begin{array}{l} \hline T \cdot \mathsf{Beh} = \mathsf{delay} \ ; \ \mathsf{C}, \quad \mathsf{t} < \mathsf{ns} \\ \hline \left[T, R, B, \mathsf{ns}, \mathsf{t}\right] & \stackrel{\mathrm{delay}}{\longrightarrow} & \left[\sigma, R, B', \mathsf{ns}, \mathsf{t}\right] \stackrel{?}{+} \delta(\mathsf{delay}) \\ T' = \langle T \leftarrow \mathsf{Beh} = \mathsf{PROG}(T) \leftarrow \mathsf{Pt} = T \cdot \mathsf{Pt} + \delta(\mathsf{delay}) \\ & \leftarrow Nd = T \cdot Nd + \mathsf{HOLDINGTIME}(T) \rangle \\ B' = B \cup \{T'\} \end{array}$$

$$\begin{array}{c} - \\ \hline \left[\sigma, R, B, \mathsf{ns}, \mathsf{t}\right] \xrightarrow{\mathrm{ud}} \left[\sigma_s, R', B', \mathsf{ns}, \mathsf{t}\right] \stackrel{}{_{+}} \delta(\mathrm{ud}) \end{array} SCUD$$

$$\begin{array}{c} B' = B \setminus \mathrm{ready}(B, \mathsf{t}) \\ R' = R \circ \mathrm{ready}(B, \mathsf{t}) \\ \mathrm{ready}(B, \mathsf{t}) = \{T \in B \mid T \cdot \mathsf{Nd} \ge t\} \end{array}$$

$$\frac{-}{\left[\sigma_{s}, a \circ R, B, \mathsf{ns}, \mathsf{t}\right] \xrightarrow{\mathrm{sa}} \left[a, R, B, \mathsf{ns}', \mathsf{t}\right] + \delta(\mathrm{sa})} SCAC$$
$$\mathsf{ns}' = \mathrm{Min}_{T \in B}(T \cdot \mathsf{Nd})$$

$$\begin{array}{c} - \\ \hline \left[\sigma_{s}, \epsilon, B, \mathsf{ns}, \mathsf{t}\right] \xrightarrow{\mathrm{si}} \left[\iota, \epsilon, B, \mathsf{ns'}, \mathsf{t}\right] \hat{+} \delta(\mathrm{si}) \end{array} SCID$$
$$\mathsf{ns'} = \mathrm{Min}_{T \in B}(T \cdot \mathsf{Nd})$$

Interrupt Handling. Rule NEWI models the arrival of a new interrupt. *I-AS* and *I-US* depict the scheduler preempting an activity and an idle task (respectively) in presence of interrupts in order to handle them. In case of arrival of interrupt during interrupt handling by the scheduler, the scheduler is restarted (transition *I-SS*). *I-IH* depicts the scheduler selecting the highest priority interrupt and inserting it at the tail of its priority list in the ready queue (all interrupt priorities are greater than all task priorities so an interrupt *will* preempt a task).

$$\frac{U \notin (\{c\} \cup R \cup IL)}{IL \rightsquigarrow [c, R, B, \mathsf{ns}, \mathsf{t}] \longrightarrow IL \circ U \rightsquigarrow [c, R, B, \mathsf{ns}, \mathsf{t}]} \quad NEWI$$

$$\frac{IL \neq \phi}{IL \rightsquigarrow [a, R, B, \mathsf{ns}, \mathsf{t}] \xrightarrow{\mathrm{as}} IL \rightsquigarrow [\sigma, a \odot R, B, \mathsf{ns}, \mathsf{t}] + \delta(\mathrm{as})} \quad I-AS$$

$$\frac{IL \neq \phi}{IL \rightsquigarrow \left[\iota, R, B, \mathsf{ns}, \mathsf{t}\right] \xrightarrow{\text{is}} IL \rightsquigarrow \left[\sigma, R, B, \mathsf{ns}, \mathsf{t}\right] \stackrel{\widehat{}}{+} \delta(\text{is})} I-IS$$

$$\begin{array}{c} IL \neq \phi \\ \hline IL \leadsto \begin{bmatrix} \sigma_s, R, B, \mathsf{ns}, \mathsf{t} \end{bmatrix} & \xrightarrow{\mathrm{ss}} & IL \leadsto \begin{bmatrix} \sigma, R, B, \mathsf{ns}, \mathsf{t} \end{bmatrix} + \delta(\mathrm{ss}) \end{array} I-SS$$

$$\begin{array}{c} - \\ \hline U \circ IL \rightsquigarrow \left[\sigma, R, B, \mathsf{ns}, \mathsf{t}\right] & \xrightarrow{\mathrm{ih}} & IL \rightsquigarrow \left[\sigma, R \circ U, B, \mathsf{ns}, \mathsf{t}\right] \stackrel{?}{+} \delta(\mathrm{ih}) \end{array} \begin{array}{c} I \text{-} IH \end{array}$$

3.6 Discussion

One of the outcomes of providing a formal semantics (of a model, language or algorithm) is that it allows to disambiguate the informal description in the natural language. One can thus formally reason about properties of the system thus described. As an example, in our semantics, we made a choice in the way the inter-dispatch time is computed. If we had strictly obeyed the Ravenscar code patterns, we would have used a modified syntax for sporadic tasks in PROGS whereby we would have made explicit the capture of the current clock from the system. We would have also had to decompose rules *RET3* and *CBCL*, introducing an additional step reflecting the capture of the current clock. A small discrepancy would then arise due to the non-atomic nature of the sporadic task release and computation of the next dispatch time, i.e., a higher priority task may preempt the sporadic task between these two actions. In case of a preemption by a higher priority task between the release of the task and the computation of the next release, a longer than stipulated inter-dispatch time may be enforced. This does not impact schedulability but can result in the sporadic tasks responding more sluggishly. This problem can be solved by assigning synchronizers the maximum priority in the system (Max_Interrupt_Priority), and returning the instance of time when the entry is executed. The maximum priority ensures that a task *cannot* be preempted while it is in the entry, thus ensuring the atomicity of the two actions. In our semantics, we chose a solution whereby the computation of the next release of sporadic tasks is performed as a side effect of the sporadic task entering the synchroniser. One may think of the scheduler performing this computation. Indeed, although the scheduler is not explicitly stated in rules rules *RET3* and *CBCL*, nevertheless, it is the scheduler which is responsible for granting control of the sporadic task when it enters the synchroniser. Thus, the scheduler performs the computation in an atomic fashion.

4 Conclusions

Previously, work has been undertaken ([8], [10], [17] and [7]) to formalize the semantics of real-time kernels and Ravenscar-like executives. In [7], the author defines an extension of CCS aimed at studying muti-tasking systems. Similarly to our approach, the general behaviour of systems made of concurrent tasks can be modeled. However, in our work, we represent the kernel functions explicitly, allowing us to account for system overhead. The work that is the closest to ours is perhaps [8] where the authors use the RTL and PVS formalisms to develop a Ravenscar-like kernel. A major difference with our contribution is that [8] aims at prescribing the development of the kernel functions whereas our contribution does provide an operational semantics which captures the global behaviour of Ravenscar systems (composed from the kernel and the running application). Another main difference with existing work is that our paper is the first direct approach at providing semantics using the structured operational semantics and not requiring any other notational support. In [11], the authors present a timed automata-based approach to the verification of Ravenscar systems.

The structured operational semantic formalization of RMM is pivotal to our tool chain as it provides to developers a direct and unambiguous description of the running behaviour of their hard real-time applications. Our semantics helped also to explicitly define the kernel functions and scheduler overheads due to context switches and interrupt handling. While the AADL is an architecture description language with open and loose semantics, our AADL to RMM transformation tool determines a rigourous semantic definition for a subset of AADL (the subset that is translatable into RMM). It must be kept in mind that the semantics given here are for executable systems generated from AADL models that are to run on a Ravenscar executive.

As stated in the introduction, with the RMM semantics we have a complete and unambiguous description of the interaction of functional code with the generated framework. This is possible due to the abstraction of functional code into the set of **PROGS** legal programs for all units. The work achieved can be usefully extended according to the approach of "semantic anchoring", whereby our operational semantics could be transposed using Abstract State Machines as a supporting anchoring language [5].

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