

A new interpolation technique for time interleaved $\Sigma\Delta$ A/D converters

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Abstract Time interleaved sigma-delta converter is a potential candidate for multi-mode wideband analog to digital (A/D) converters dedicated for multistandard receivers. However, the interpolation by zeros to compress the useful signal bandwidth at the input of the sigma-delta modulator imposes constraints on the implementation of the analog part leading to a very large die area due to the high value required for the sampling capacitor. This paper proposes a new interpolation technique using extra samples instead of zeros resulting from the oversampling of the input signal. This new technique not only reduces the die area and the order of the anti-alias filter but also improves A/D converter performance. The proposed technique was simulated and implemented in a four channel time interleaved sigma-delta designed in a 1.2 V 65 nm CMOS process.

Keywords Sigma-delta · Analog-to-digital conversion · Interpolation · Time-interleaving

1 Introduction

The current evolution of telecommunication systems moves toward versatile, reconfigurable and multistandard receiver. In this context, the concept of software radio [1] and cognitive radio [2] presents an interesting solution to reach these requirements allowing optimal management of the frequency resources in the radio environment and introducing the dynamic reconfiguration for multistandard applications. In the radio frequency (RF) frontend of the receiver, the main idea consists of moving the A/D converter as near as possible to the antenna. The A/D converter suitable for this application must be capable of a bandwidth-resolution exchange to ensure multistandard reception while maintaining low power consumption.

Widening the conversion bandwidth of the A/D converters while ensuring high resolution remains a bottleneck to overcome. Sigma-delta ($\Sigma\Delta$) converters [3] are good candidates to achieve high resolution conversion but their bandwidth is very narrow compared to the requirements needed for software radio applications.

To overcome this problem, several research works have been developed employing parallelism to widen the bandwidth of the $\Sigma\Delta$ A/D converters: frequency band decomposition (FBD) [4, 5], Parallel sigma-delta ($\Pi\Sigma\Delta$) [6], and two techniques of Time Interleaved sigma-delta (TI $\Sigma\Delta$) [7–12]. The major benefit of all of these approaches is that they increase the conversion bandwidth with a linear increase of the power consumption whereas with a single sigma-delta modulator, the power consumption increases exponentially while drastically increasing the bandwidth [13].

FBD architecture uses bandpass $\Sigma\Delta$ modulators equally distributed in the useful band. This architecture is adapted to heterodyne receivers and is very robust to analog

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mismatch. However, it is the most complex because it needs the implementation of different bandpass sigma-delta modulators.

The $\Pi\Sigma\Delta$ solution based on Hadamard modulation requires less hardware complexity since it uses the same $\Sigma\Delta$ modulator for all channels but it needs high order digital filters to achieve the theoretical performance. On the other hand, achieving a high resolution using this technique requires the use of a large number of channels which makes it unsuitable for the desired application.

The $TI\Sigma\Delta$ solution proposed in [7, 8], known also as block filtering (BF) $\Sigma\Delta$, has also the advantage of using the same modulator for all channels. Moreover, the digital resources needed for signal demultiplexing and signal reconstruction are very low. However, this technique suffers from a main drawback. In fact, to achieve the desired noise transfer function, the i th integrator output of each channel must be applied to the input of all channels' i th + 1 integrators with an appropriate gain and delay. These inter-channels signals cause a layout complexity increase, additional mismatch and couplings specially if the number of channels and integrators per channel is large.

The second $TI\Sigma\Delta$ solution proposed in [9–12] uses as well the same modulator for all channels and requires reasonable digital resources for signal demultiplexing and signal reconstruction [14]. Besides, no analog signals need to travel between channels which eliminates the modulator architecture and the number of channels constraints from which the first solution suffers.

The main challenge in the implementation of this architecture lies in securing a high resolution. In fact, the interpolation required to compress the useful signal bandwidth at the input of the sigma-delta modulator is carried out by inserting zeros between every two adjacent samples of the input signal sampled at the Nyquist rate. As a consequence, the useful signal power is decreased and

therefore to maintain the same signal power to thermal noise power ratio, high values for sampling capacitor are needed.

To overcome this problem, this paper presents a new interpolation technique based on oversampling the input signal to considerably reduce the capacitor size. This technique was validated in a four channel $TI\Sigma\Delta$ A/D converter designed in a 1.2 V 65 nm CMOS process whose specifications are given in [15, 16].

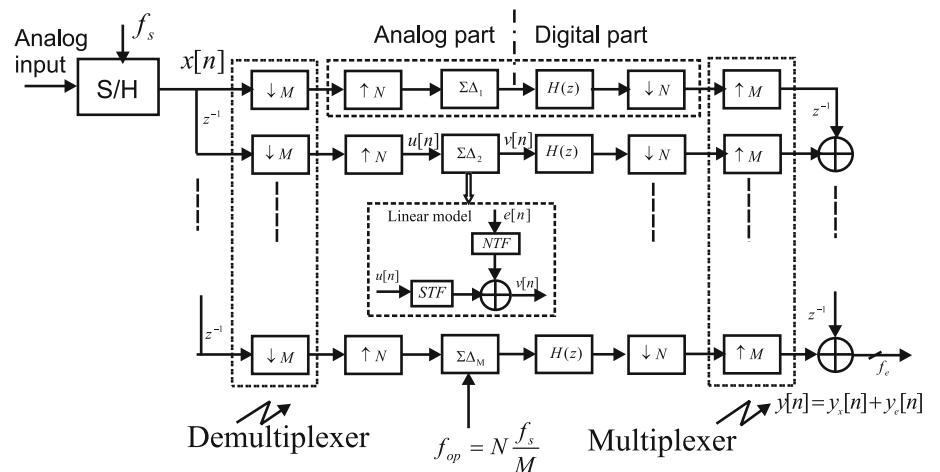
The second section of this paper describes the principle of $TI\Sigma\Delta$ A/D converters and the digital filters required for the reconstruction of the useful signal. Section 3 presents the implementation constraints of the analog components of the $TI\Sigma\Delta$ A/D converter. Section 4 sheds light on the new interpolation technique for reducing implementation constraints and on its impact on the digital processing. In Sect. 5, the implementation of the new interpolation technique is presented and the performance of this technique is evaluated using a four channel $TI\Sigma\Delta$ A/D converter prototype presented in Sect. 6. Finally, the last section concludes with an evaluation of the complexity and the performance of the proposed interpolation technique.

2 Time interleaved sigma-delta architecture

2.1 Principle

The simplified schematic of a $TI\Sigma\Delta$ A/D converter is depicted in Fig. 1. The architecture is composed of M parallel low-pass $\Sigma\Delta$ modulators. The analog input signal is sampled at the Nyquist rate f_s . Then, the signal $x[n]$ is distributed among the M modulators through an analog multiplexer and interpolated by a factor N to compress the useful signal bandwidth. The signal then goes through the $\Sigma\Delta$ modulator and the quantization noise shaping is carried

Fig. 1 $TI\Sigma\Delta$ ADC architecture



out. Afterwards, the output of each modulator is filtered by the digital filter $H(z)$ to suppress the out of band quantization noise. Finally, the signal is decimated by a factor N to reduce the data rate before being demultiplexed by a digital demultiplexer to reconstruct the output signal $y[n]$.

Relying on the linear model of the modulator shown in figure, the overall output of the $TI\Sigma\Delta$ A/D converter $y[n]$ is the sum of the overall signal components $y_x[n]$ and the overall quantization error components $y_e[n]$:

$$y[n] = y_x[n] + y_e[n] \quad (1)$$

The overall signal component is just a delayed version of the input signal (2) [6] if the digital filter coefficients of $H(z)$ satisfy the condition (3).

$$Y_x(z) = z^{-(M-1-L)}X(z) \quad (2)$$

$$h[n] = \begin{cases} 1 & n = (L-1)/2, \quad L : \text{is the filter length} \\ 0 & \text{where } (n - \frac{L-1}{2}) \text{ is multiple of } N \end{cases} \quad (3)$$

The theoretical signal to noise ratio (SNR) of a $TI\Sigma\Delta$ A/D converter depends on three parameters: the order of the modulators (P), the number of quantizer levels inside the modulator loop and the interpolation factor (N). The conversion bandwidth depends on the number of channels (M). The number of taps in digital filters (L) determines the hardware complexity needed to reach the expected SNR.

The architecture of the sigma-delta modulator implemented in [15] is a fourth order General Multi Stage Closed Loop (GMSCL) [17] with 2.5 bits level DAC (Fig. 2). This structure will be employed in all system simulations. Its advantage is that it does not need digital pre-filtering to cancel first stage quantization noise as is the case in traditional cascade sigma-delta. Modulator coefficients are chosen as a compromise between modulator stability, suppression of quantization noise, unity signal transfer function (STF) and maximum hardware reusability [18].

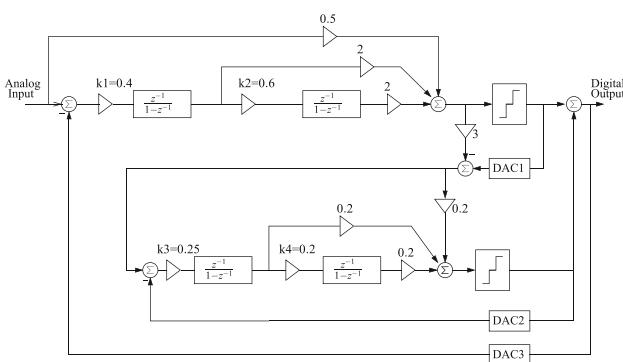


Fig. 2 GMSCL sigma-delta struture

2.2 Digital filter

An optimal filter topology which fulfills the perfect reconstruction constraints (3) was proposed in [6]. The other coefficients not expressed in (3) are calculated in order to minimize the quantization noise power at the output of the $TI\Sigma\Delta$ A/D converter. It has been shown in [14] that a 310th order optimal low-pass filter is required to reach an SNDR of 81 dB. This filter length requires the implementation of 155 multiplications and 300 additions operating at the operating frequency f_{op} . This is a very huge computing resource requirement.

In order to reduce hardware complexity, a new digital reconstruction method based on Comb-filters was proposed in [14]. The Comb-filters can operate at high sampling rates while minimizing hardware complexity. The transfer function $C(z)$ of a Comb-filter is defined by:

$$C(z) = \left(\frac{1}{N} \sum_{i=0}^{N-1} z^{-i} \right)^{K_f} = \left(\frac{1}{N} \frac{1-z^{-N}}{1-z^{-1}} \right)^{K_f} \quad (4)$$

where K_f and N are the order of the Comb-filter and the decimation ratio respectively.

According to Eq. 4, a Comb-filter can be efficiently implemented using only integrators and differentiators as shown in Fig. 3. However, its impulse response does not satisfy the perfect reconstruction conditions in (3). The overall output signal component is not a delayed version of the input signal. It is a filtered version as shown in the following equation:

$$Y_x(z) = H'(z^M)z^{-(M-1-L)}X(z) \quad (5)$$

where

$$H'(z) = \sum_{i=d}^J h_c[iN]z^{-i} \quad \text{with} \quad JN \leq P \quad (6)$$

with $h_c[n]$ is the impulse response of the Comb-filter and d the decimation delay of the impulse response $h_c[n]$.

The filtering effect ($H'(z^M)$) appears as equiripples on the magnitude of the output spectrum. To correct this effect, an equalization filter $F(z)$ is applied at the output of the $TI\Sigma\Delta$ A/D converter based on a least mean square (LMS) FIR filter. The order of this equalization filter depends on the equiripple magnitudes introduced by $H'(z^M)$ and the equiripple magnitude depends on both the order of the Comb-filter and on the decimation delay d . It has been shown in [14] that, for a P th order $\Sigma\Delta$ modulator, the optimal

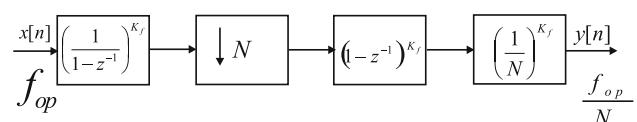


Fig. 3 Comb-filter architecture

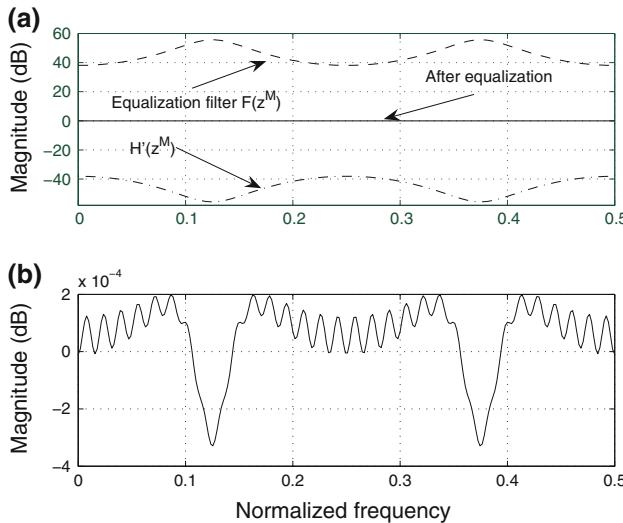


Fig. 4 **a** Magnitude of $H'(z^M)$ transfer function and equalization filter $F(z^M)$, **b** zoom of the magnitude error after equalization

Comb-filter order reducing aliasing terms (due to the decimation) and equalization filter complexity must be the first even number higher than $P + 1$ with zero delay.

Figure 4 shows the magnitude response in dB of $H'(z^M)$, $F(z)$ and the result of equalization. For a sixth order Comb-filter, the ripple magnitude is about 14 dB so a 30th order equalization filter is enough to equalize ripples with a maximum error of 3×10^{-4} dB. While for a 2 dB inband ripple magnitude, a tenth order equalization filter is enough.

3 Analog implementation

Figure 5 shows one way to implement the front-end of a $TI\Sigma A/D$ converter using switched capacitor (SC) technology. For the sake of simplicity, a single-ended representation is illustrated. In Fig. 5, the S/H and the first channel analog multiplexer and the first integrator are illustrated. The S/H was placed before all channels to avoid clock-skew. Other techniques such as global passive sampling [19] and clock calibration [20] can be used instead but they may not be as efficient as the S/H approach.

As shown in Fig. 5, an analog multiplexer is placed between the S/H and the first integrator of all channels. It consists of just two switches: the first one processes signal samples and the other one is connected to the common mode to acquire zero values. The clock signals that control the multiplexer, ϕ_{i-SSd} and ϕ_{i-ZSd} , are generated in the interpolation network that will be discussed later in Sect. 5. This network generates clock signals that perform the decimation by M and the interpolation by N , just before the modulator as shown in Fig. 1. The other clock signals are represented in Fig. 5. The delayed versions of the clocks are employed for the bottom plate sampling technique that decreases the charge injection and makes it signal independent [21].

One of the advantages of the $TI\Sigma A/D$ converter is the capacity to perform a Nyquist conversion. However, in high resolution applications, it requires very high value of sampling capacitors because the thermal noise must be lower than the quantization noise defined by the converter

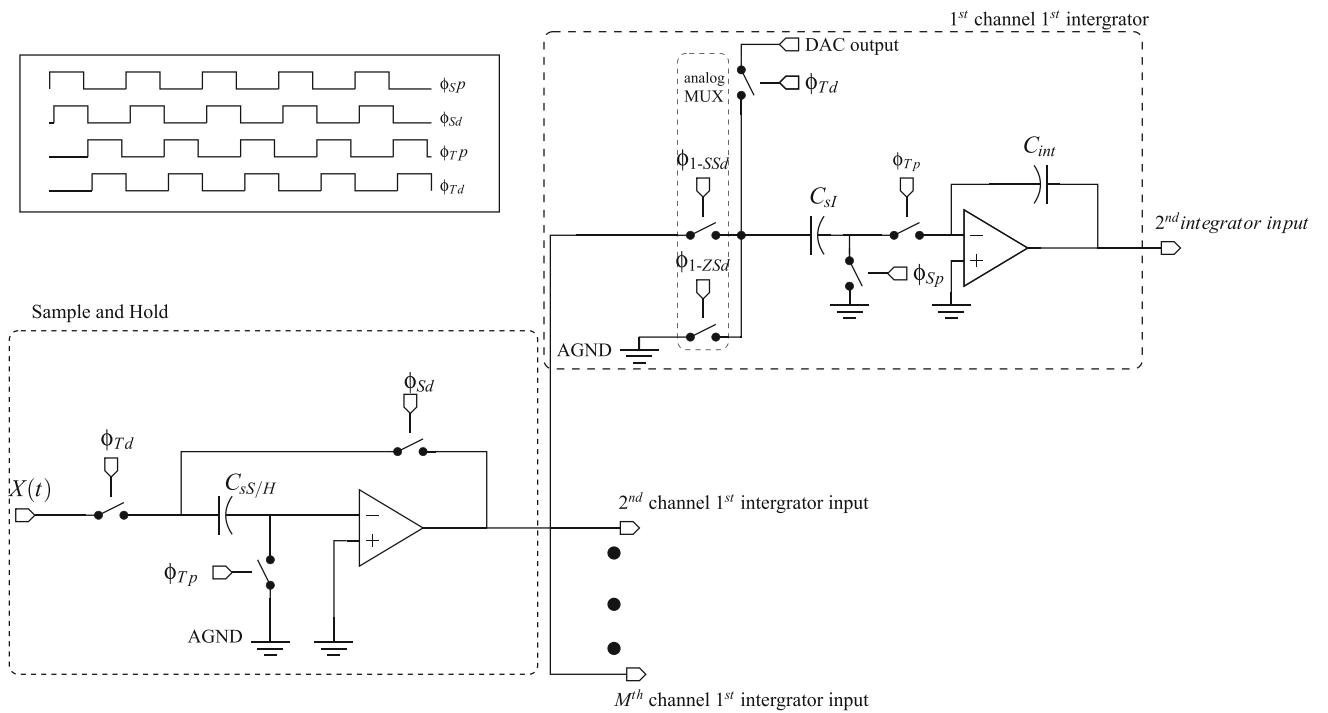


Fig. 5 $TI\Sigma A/D$ circuit front-end

resolution. Therefore, the sampling capacitor $C_{SS/H}$ of the S/H and C_{sI} of the first integrator are sized to get the thermal noise level lower than the expected resolution. Let $\text{SNR}_{\text{required}}$ be the required signal to noise ratio (SNR) for the converter, P_s the signal power and P_{th} the thermal noise power, then

$$10 \log \left(\frac{P_s}{P_{th}} \right) > \text{SNR}_{\text{required}} \quad (7)$$

where

$$P_{th} = \frac{4K_{Bol}T}{C} \quad (8)$$

$$P_s = \frac{A^2}{2} \quad (9)$$

with K_{Bol} the Boltzman constant, T the temperature in Kelvin and with A the sinusoidal input signal amplitude.

This give us:

$$C_{SS/H} > \frac{8K_{Bol}T \cdot 10^{\text{SNR}/10}}{A^2} \quad (10)$$

At the input of the $\Sigma\Delta$ modulator, the signal is oversampled by a factor N and if the digital filter removes the out of band noise without any amplification, the effective thermal noise power will be then reduced by a factor N . On the other hand, since the interpolation is performed by adding zeros, and the digital filter has no amplification gain, the signal power is decreased by N also.

$$P_{th} = \frac{4K_{Bol}T}{C \cdot N} \quad (11)$$

$$P_s = \frac{A^2}{2 \cdot N} \quad (12)$$

It results in

$$C_{sI} > \frac{8K_{Bol}T \cdot 10^{\text{SNR}/10}}{A^2} \quad (13)$$

For example, for a UMTS scenario using two channels with an normalized input signal amplitude of 0.35 V and an expected SNR of 83 dB at 300 Kelvin, the sampling capacitors are 54 pF which consume an unreasonable die area.

4 The new interpolation technique

4.1 Principle

In order to overcome the disadvantages of classical $TI\Sigma\Delta$ A/D converter, the solution proposed in this paper consists in oversampling the input signal of the bank of modulators at the operation frequency $f_{op} = \frac{N}{M}f_s$ where f_s is the Nyquist sampling frequency. Then, extra samples behind each

“Nyquist sample” (obtained with Nyquist sampling rate) will be used instead of zeros in the interpolation by a factor N . The added extra samples will increase the signal power and consequently allows to reduce the sampling capacitor size while maintaining the same signal power to thermal noise power ratio.

The number of inserted samples N_s at each channel varies between 0 and $N - 1$. Figure 6 shows an explicit example of the new interpolation technique with $M = 2$, $N = 12$ and $N_s = K - 1$ where K is the ratio defined by $K = \frac{N}{M}$. The dashed vertical lines represent the samples obtained at the Nyquist rate (“Nyquist samples”) and multiplexed in time between the two channels. The sampling at f_{op} (Fig. 6a) creates $(K - 1)$ extra samples between two adjacent “Nyquist samples” (5 in this example). The interpolation with the classical technique is performed by inserting $N - 1$ zeros between “Nyquist samples” at the input of the modulator (Fig. 6b). Meanwhile, the interpolation with the proposed technique uses the $K - 1$ extra samples after each “Nyquist sample” and completes the rest with zeros to reach the $N - 1$ values to perform the interpolation by N (Fig. 6c, d).

To evaluate the theoretical performance, Fig. 7 presents the equivalent mathematical model of the $TI\Sigma\Delta$ A/D converter using the proposed interpolation technique. The transfer function $F_i(z)$ presents the effect of the new interpolation on the input signal $X(z)$ in the i th channel before the $\Sigma\Delta$ modulator. Figure 9 shows in details the

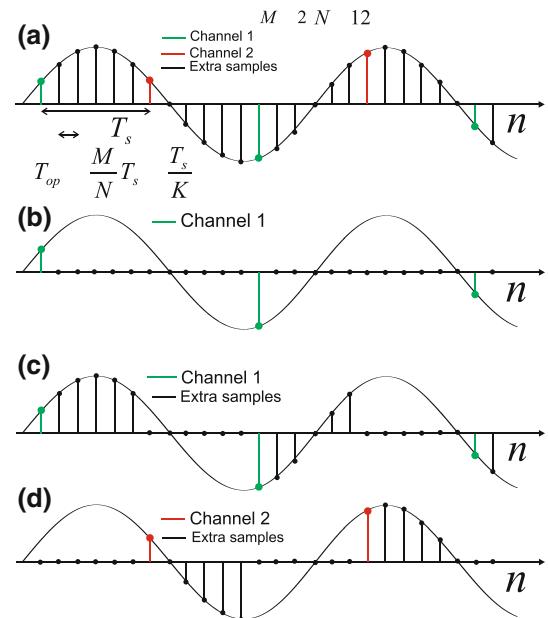


Fig. 6 Example illustrating the new interpolation technique. **a** Input signal sampled at the operation frequency f_{op} , **b** input signal at channel 1 with the interpolation by zeros, **c**, **d** input signals at the channels 1 and 2 with the new interpolation technique with $N_s = K$ extra samples

structure of $F_i(z)$ where N_s samples are used. For the example presented in Fig. 6, Fig. 8 shows the different steps to built the signal of the first channel. Based on this simple example, we could define the general form of $F(z)$ for the i th channel as presented in Fig. 9.

Fig. 7 Mathematical model of the $TI\Sigma\Delta$ architecture with the new interpolation technique

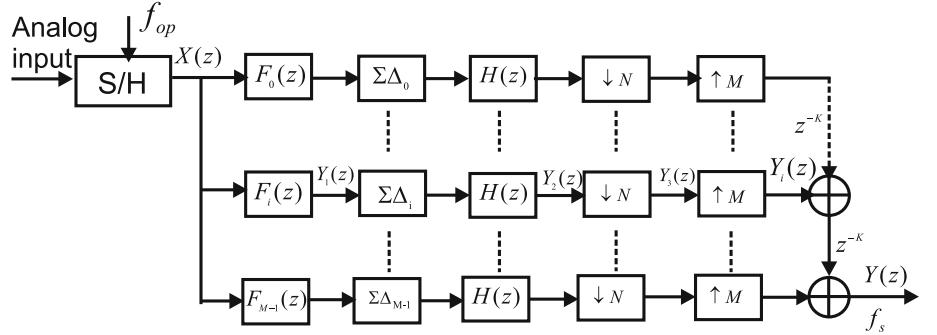
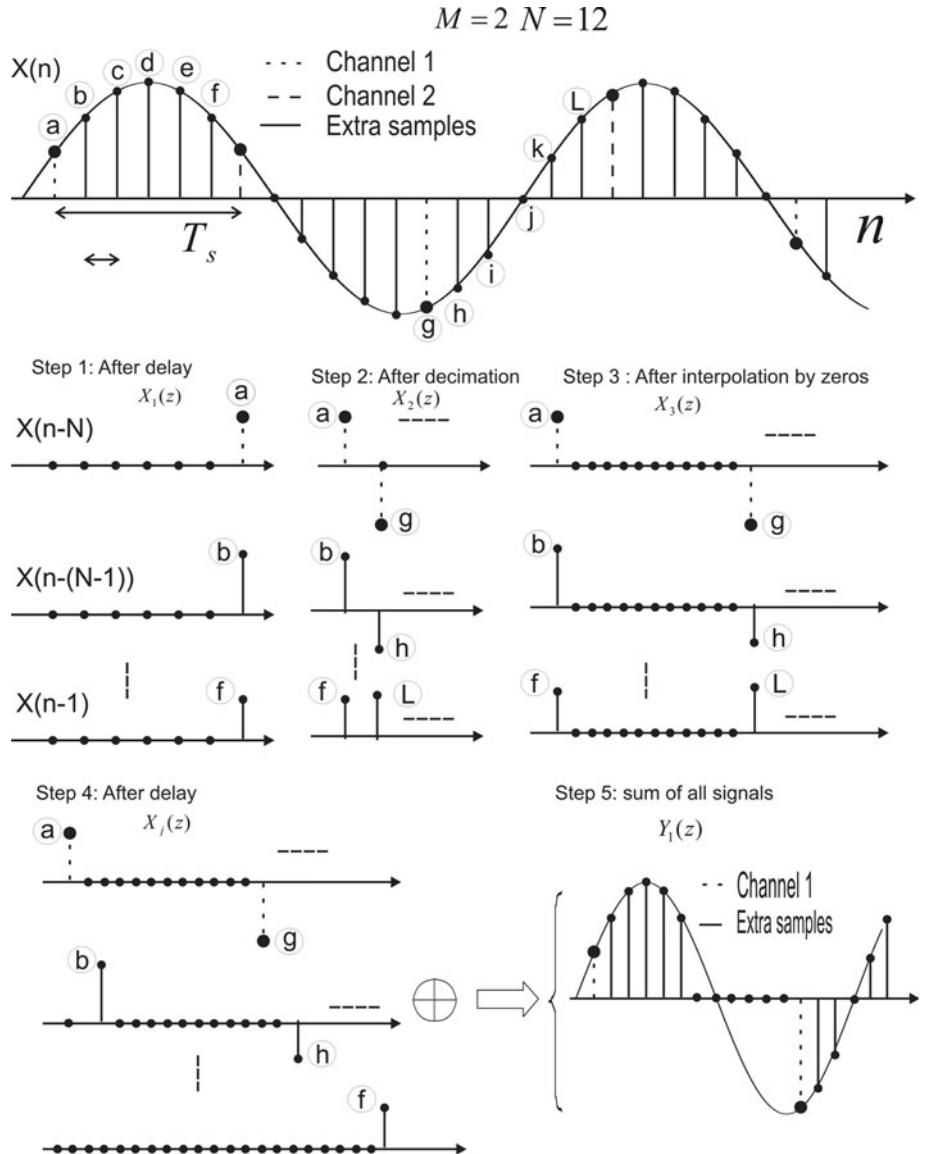


Fig. 8 The different steps for the construction of the signal of the first channel



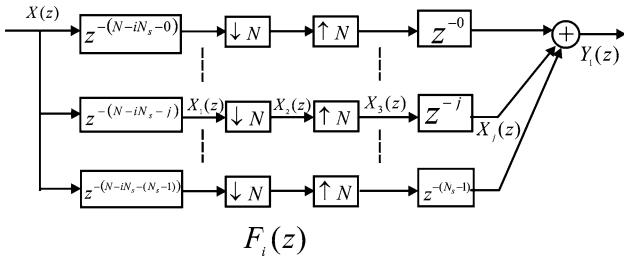


Fig. 9 Transfer function $F_i(z)$

reconstructing the output signal. The different intermediate signals and the output $Y_1(z)$ can be expressed by:

$$X_2(z) = X_1(z)|_{\downarrow N} = \frac{1}{N} \sum_{l=0}^{N-1} X_1(z^{\frac{l}{N}} W_N^l);$$

$$W_N = e^{-j\frac{2\pi}{N}} = z^{\frac{-(N-iN_s-j)}{N}} \frac{1}{N} \sum_{l=0}^{N-1} W_N^{-l(N-iN_s-j)} X(z^{\frac{l}{N}} W_N^l) \quad (14)$$

$$Y_1(z) = \sum_{j=0}^{N_s-1} z^{-j} X_3(z) = \sum_{j=0}^{N_s-1} z^{-j} X_2(z^N)$$

$$= z^{-(N-iN_s)} \sum_{j=0}^{N_s-1} \frac{1}{N} \sum_{l=0}^{N-1} W_N^{-l(-iN_s-j)} X(z^N W_N^l) \quad (15)$$

Relying on the linear model of the modulator shown in Fig. 1 and assuming that the signal transfer function of the $\Sigma\Delta$ modulator is a pure delay, the useful signal $Y_1(z)$ is filtered by the digital filter $H(z)$ before being decimated by N and interpolated by M . The following expressions describe mathematically these different operations:

$$Y_3(z) = Y_2(z)|_{\downarrow N} = \frac{1}{N} \sum_{p=0}^{N-1} Y_2(z^{\frac{p}{N}} W_N^p) \quad (16)$$

$$Y_i(z) = Y_3(z)|_{\uparrow M} = Y_3(z^M) = \frac{1}{N} \sum_{p=0}^{N-1} Y_2(z^{\frac{M}{N}} W_N^p) \quad (17)$$

Finally, the expression of the output $Y(z)$ is given by Eq. 18. This equation is very hard to simplify. It is thus very difficult to analytically evaluate the impact of the proposed interpolation technique on the overall performance of the converter and the complexity of the

digital filter. In order to complete our study, the choice of the Comb-filter on each channel will be kept due to its implementation simplicity (Sect. 2.2). Then, simulations will be performed to estimate the impact of the new interpolation on the performance of the whole system and the hardware complexity of the equalization filter $F(z)$ at the output (Sect. 2.2).

4.2 Simulation results

The number of inserted samples N_s controls the dynamic range of the converter, the SNDR and the complexity of the equalization filter which must ensure good equalization of the ripples without introducing a large amplification of the quantization noise.

The main factor controlling the performance and the hardware complexity is the ripple magnitude due to filtering effects introduced by the Comb-filters. In fact, the higher the ripple magnitude, the higher the order of the equalization filter and the higher the amplification of the quantization noise. To estimate the ripple magnitude, a sine cardinal signal is used at the input of the $T/I\Sigma\Delta$ A/D converter due to its constant power spectral density (PSD) throughout the useful band. A four channel $T/I\Sigma\Delta$ A/D converter with interpolation factor of 80 was considered to perform system simulations.

Figure 10 shows the PSD of the signal $X(Z)$ sampled at the frequency f_{op} . Figure 11 shows the PSD of the signal $Y(Z)$ for different values of N_s and Fig. 12 shows the ripple magnitude with respect to the number of inserted samples N_s for two different values of interpolation factor N . It can be noticed that:

- the ripple magnitude reaches its maximum value for N_s equal to $\frac{N}{2} - 1$ and $N - 1$,
- the maximum value for N_s increasing the power of the useful signal with no large ripple magnitude is equal to $K - 1$. This implies that the optimal case is first to perform the interpolation in each channel by adding extra samples resulting from oversampling until the next “Nyquist sample” dedicated to the adjacent channel, then, to continue the interpolation by adding zeros (Fig. 6c).

$$Y(z) = \sum_{i=0}^{M-1} z^{-iN_s} Y_i(z) = z^{-M} \sum_{i=0}^{M-1} z^{-(N_s-1)i} \left[\frac{1}{N} \sum_{p=0}^{N-1} \left[W_N^{-p(N-iN_s)} \sum_{j=0}^{N_s-1} \frac{1}{N} \sum_{l=0}^{N-1} W_N^{-l(-iN_s-j)} X(z^{N_s} W_N^{l+p}) \right] H(z^{N_s} W_N^p) \right] \quad (18)$$

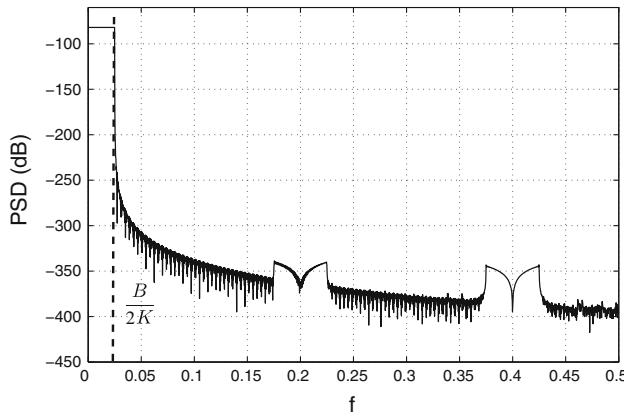


Fig. 10 Power Spectral Density of the input signal sampled at f_{op} with $NBW = \frac{0.5}{80000}$

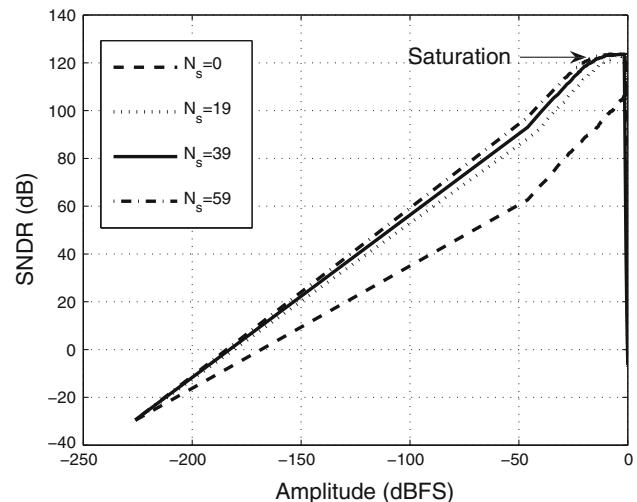


Fig. 13 SNDR with respect to the input signal magnitude for different inserted samples

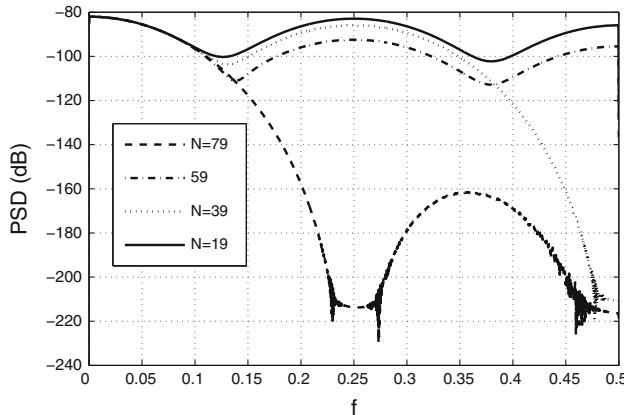


Fig. 11 PSD at the output for different values of N_s with a sine cardinal signal at the input with $NBW = \frac{0.5}{80000}$

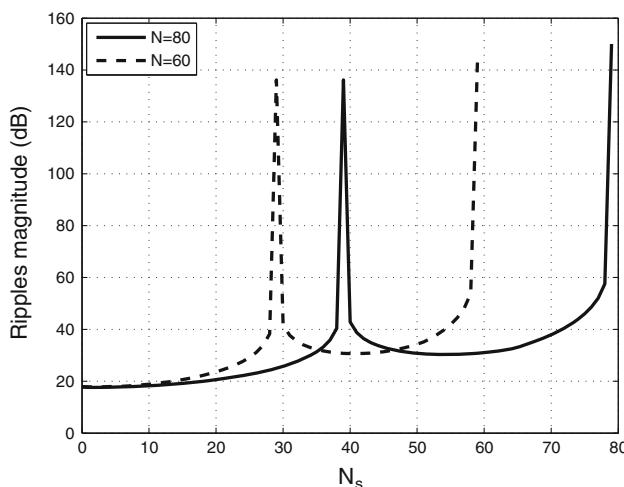


Fig. 12 Ripple magnitude on the PSD at the output respect to N_s for the two interpolation factor $N = 80$ and $N = 60$

On the other hand, the new interpolation technique increases the power of the useful signal on each channel and may saturate the integrators inside the sigma–delta modulator. Figure 13 shows the SNDR with respect to the amplitude of the input signal for different values of inserted samples N_s .

The value $N_s = 0$ corresponds to the case of interpolation technique by zeros. It can be easily noted that interpolating with extra samples improves the SNDR. This result is expectable because increasing N_s increases the useful signal power and consequently the SNDR. However, increasing N_s increases also integrators' swings and thus the maximum stable amplitude is reduced. To avoid this problem, a decrease of the integrators' coefficients could ensure a linearly dynamic range and maintain the expected maximum SNDR. Figure 14 shows the SNDR compared to the input signal magnitude for different values of N_s with two sets of gain integrators. The set with lower integrator gain allows a wide linear dynamic range at the cost of a slight decrease in the SNDR.

4.3 Equalization filter complexity

After determining the optimal number of inserted samples N_s , let us estimate the complexity of the equalization filter. Indeed, the equalization filter equalizes the filtering effect introduced by the Comb-filter whereas it amplifies the quantization noise at the output leading to a small loss of the SNDR. An inband ripple magnitude of 2 dB is tolerated. The optimal order of the equalization filter must ensure magnitude ripples lower than this value without large amplification of the quantization noise. Figure 15 shows the SNDR and the magnitude ripples with respect to

Fig. 14 SNDR with respect to the input signal magnitude for different inserted samples with two sets of gain integrator

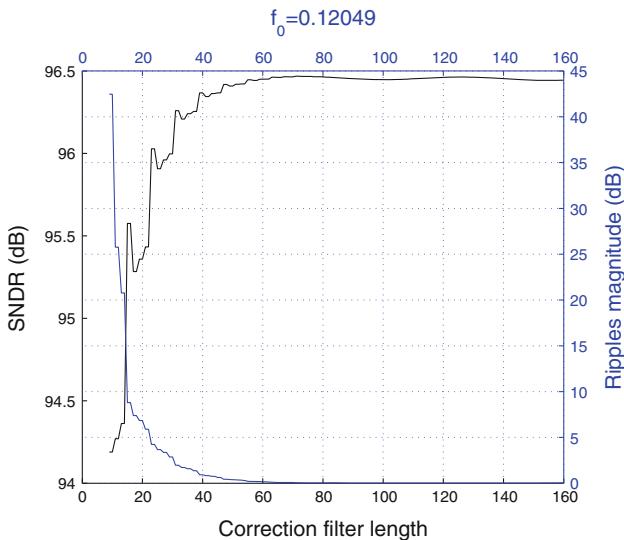
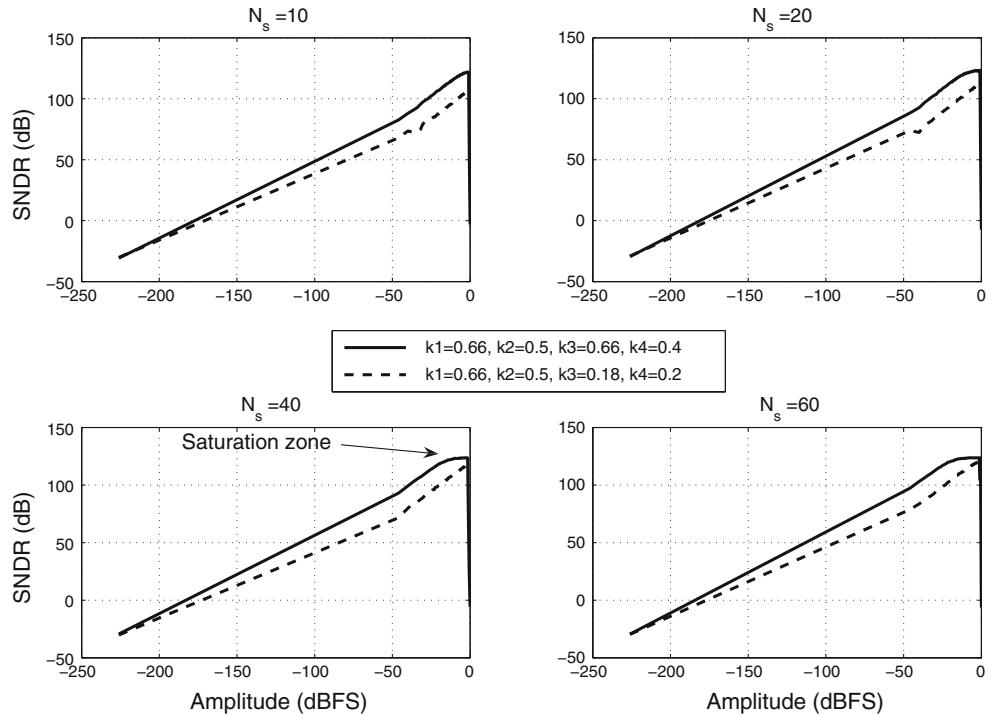


Fig. 15 SNDR and magnitude ripples after equalization compared to equalization filter length

the equalization filter length. The SNDR was estimated using a sine signal at the input located at the frequency for which the attenuation introduced by the filtering effect reaches its maximum value. It can be noticed that a 30th order equalization filter is sufficient to have magnitude ripples less than 2 dB and an SNDR of 95 dB.

To illustrate the equalization filter effect, Fig. 16 shows the power spectral densities at the output, before and after equalization, while considering a sine wave signal at the

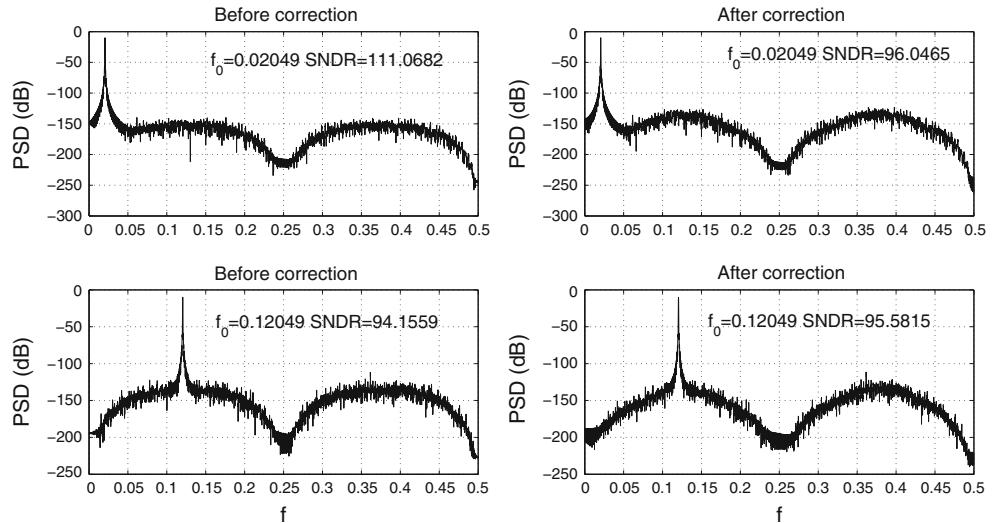
input at the normalized frequency f_0 . It can be noticed that:

- for a low normalized frequency ($f_0 = 0.02$) the SNDR before equalization is equal to 111 dB. There is no attenuation at low frequencies by the filtering effect and thus the expected SNDR is maintained. After the equalization filter, the SNDR is reduced to 96 dB because the equalization filter does not amplify the useful signal while amplifying the quantization noise.
- for the normalized frequency $f_0 = 0.12$, the SNDR before equalization is equal to 94 dB. This is because the attenuation introduced by the filtering effect reaches its maximum value at this frequency. The SNDR will be slightly improved to 95.5 dB after the equalization filter. In this case, the equalization filter amplifies the useful signal and the quantization noise at the same time that regaining the useful signal amplitude and introducing a slight improvement of the SNDR. after the equalization filter, the SNDR is almost constant (96 dB) regardless of the frequency of the input signal.

4.4 Choice of the sampling frequency

The new interpolation technique has been exposed to a rise of the sampling frequency from f_s to f_{op} . It decreases the sampling capacitor size by a factor of K . In fact, with the new interpolation technique, Eqs. 8 and 12 become respectively:

Fig. 16 Power spectral density at the output before and after equalization with a sine signal at the input with $NBW = \frac{0.5}{2^{17}}$



$$P_{th} = \frac{4K_{bol}T}{C \frac{f_{S/H}}{f_s}} \quad (19)$$

$$P_s = \frac{A^2}{2N} \frac{f_{S/H}}{f_s} \quad (20)$$

And since the S/H power signal (Eq. 9) and the integrator thermal noise power (Eq. 11) remain the same, the capacitor size for both of them can be divided by $\frac{f_{S/H}}{f_s}$ (which is equal to K if $f_{S/H} = f_{op}$) while maintaining the same signal to thermal noise ratio.

Besides, other S/H sampling frequencies can be considered. Figure 17 shows the proposed interpolation technique for a sampling frequency of $f_{op}/2$. In this scenario,

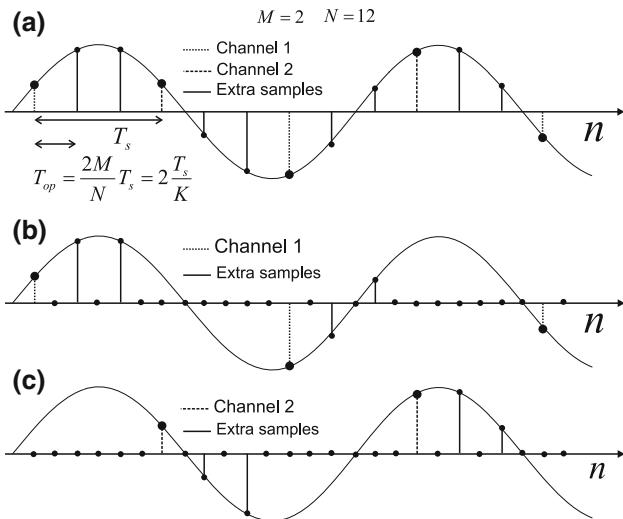


Fig. 17 Example illustrating the new interpolation technique. **a** Input signal sampled at the operation frequency $f_{op}/2$, **b**, **c** input signals at the channels 1 and 2 with $N_s = K/2$

since the sampling operation requires $2T_{op}$, the number of available extra samples between two “Nyquist samples” will be reduced compared to the case where the sampling frequency is f_{op} . The interpolation by N is performed in the same way as described in Sect. 4.1 by using the available extra samples between two “Nyquist samples” and by inserting the appropriate number of zeros to achieve an increase of the data rate by N factor (see Fig. 17).

In this case, the signal power increase and consequently the sampling capacitor decrease will not be as high as when sampling at f_{op} but it could relax the constraints design of S/H. These constraints do not increase as it can be supposed with $f_{S/H}$ increase. In fact, explained before, each time $f_{S/H}$ is multiplied by a certain factor, the sampling capacitor can be divided by the same factor while maintaining the same signal to thermal noise ratio. Consequently, the OTA slew rate and gain bandwidth will be almost multiplied by the same factor and therefore their ratio to $f_{S/H}$ will remain unchanged. As a consequence, the distortions generated due to settling error will also remain unchanged [22]. As for the switches’ charge injection, its effect is reduced by the use of the bottom plate sampling technique. Meanwhile, jitter, thermal, flicker and other noises preserve the same impact and even for some of them the impact is reduced when $f_{S/H}$ increases due to the fact that out of band noise is eliminated by the $\Sigma\Delta$ decimation filter [23].

Another important advantage of this novel interpolation technique is reducing the complexity of the anti-alias filter (AAF). In order to show this complexity reduction, let us consider the digitization of a UMTS channel using a Zero-IF architecture. The spectrum of the useful signal and of the adjacent channels at the input of the A/D converter are shown in Fig. 18. If the classical technique is employed, the adjacent channels will alias inside the useful band and

thus their amplitude after filtering should be lower than the quantum of the A/D converter. Therefore, we should have:

$$P_{block} < P_{signal} - ADC_{res}$$

where P_{block} is the power in dB of the blockers after filtering, P_{signal} the power in dB of the useful signal and ADC_{res} is the targeted resolution in dB. In the considered scenario, to fulfill this condition, a 20-th order butterworth filter is required that in addition to its complexity adds a 4 dB inband attenuation that should be corrected in the digital baseband. On the other hand, for the proposed interpolation technique, the adjacent channels just reduces the dynamic range of the A/D converter. Consequently, the required attenuation for the blockers is significantly lower. For example, to have the power of the blockers after filtering equal to 1% the power of the useful signal which just causes 0.01 dB reduction of dynamic range, a sixth order AAF is required.

5 Interpolation network implementation

To validate the proposed interpolation technique, a reconfigurable clock generation circuit (Fig. 19) that will be referred to as the interpolation network has been designed. It generates the analog multiplexer clock signals for a given N, M and S/H sampling frequency. Four different S/H sampling frequencies can be achieved: f_{op} , $f_{op}/2$, $f_{op}/4$ and $f_{op}/8$. The implemented interpolation network operation is based on the common tokenring. Each channel has N_D D-flipflops. These flipflops are placed in series and connected to each others via tri-state cells. The tri-state cell control signals $K_{1..N_D}$ set the number of flipflops that see the token equal to K . Moreover, the channel flipflop chains are also placed in series and are connected together via another tri-state cell. Its control M_i enables or disables the next channel.

In the meantime, the flip-flop outputs $D_{i,j}$ are recovered in OR networks to generate multiplexers' clock signals

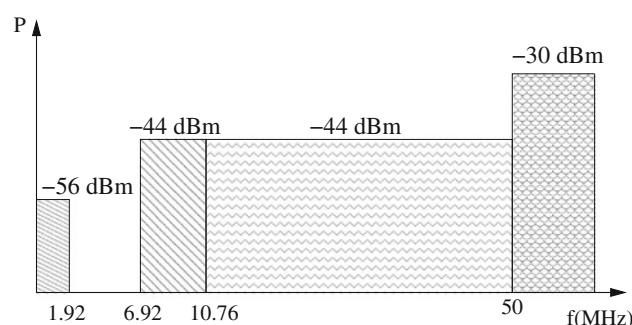


Fig. 18 Worst case blocking signals for a UMTS scenario

ϕ_{i-SSd} and ϕ_{i-Zsd} . At ϕ_{i-SSd} clock front, a signal sample is processed and at ϕ_{i-Zsd} clock front, samples of value ‘zero’ are obtained. As said before, when sampling at f_{op} , the first channel performs its interpolation by a factor N by adding the first K signal samples followed by $N - K$ zeros. Meanwhile when sampling at $f_{op}/2$, $K/2$ samples are acquired during $K.T_{op}$. Therefore, the even samples are replaced by zeros. Similarly, the modulo 2 to 4 signal samples when sampling at $f_{op}/4$ and the modulo 2–8 signal samples when sampling at $f_{op}/8$, are replaced by zeros.

To create these clock signals, the modulo 8 flip-flop outputs of each channel are firstly ORed together:

$$OR_{i,j} = \sum_{k=0}^3 D_{i,(j+8k)} \quad (21)$$

For example, the OR output of $(D_{1,1}, D_{1,9}, D_{1,17} \text{ and } D_{1,25})$ will be referred to as $OR_{1,1}$, $(D_{1,2}, D_{1,10}, D_{1,18} \text{ and } D_{1,26})$ as $OR_{1,2}$ and so on. The four clock signals are generated as follows:

- For a sampling frequency of $f_{op}/8$, the i th channel ϕ_{i-SSd} is given by:

$$f_{op}/8\phi_{i-SSd} = OR_{i,1} \bullet \phi_{Sd}$$

In fact, the token reaches $D_{1,9}$ eight T_{op} after reaching $D_{1,1}$ creating thereby a clock signal having a front every eight T_{op} . This will allow us to get the signal samples every eight T_{op} as desired

- For a sampling frequency of $f_{op}/4$, the i th channel ϕ_{i-SSd} is given by:

$$f_{op}/2\phi_{i-SSd} = (OR_{i,1} + OR_{i,5}) \bullet \phi_{Sd}$$

- For a sampling frequency of $f_{op}/2$, the i th channel ϕ_{i-SSd} is given by:

$$f_{op}/4\phi_{i-SSd} = (OR_{i,1} + OR_{i,3} + OR_{i,5} + OR_{i,7}) \bullet \phi_{Sd}$$

- For a sampling frequency of f_{op} , the i th channel ϕ_{i-SSd} is given by:

$$f_{op}\phi_{i-SSd} = \sum_{k=1}^8 (OR_{i,k}) \bullet \phi_{Sd}$$

The \bullet and the $+$ stand for an AND and OR operations respectively. During sampling phases, the integrator sampling capacitor must either store signal samples or zeros therefore ϕ_{i-Zsd} is the conjugate of ϕ_{i-SSd} when ϕ_{Sd} is high. Its expression is given by:

$$\phi_{i-Zsd} = \bar{\phi}_{i-SSd} \bullet \phi_{Sd}$$

Figure 20 shows the four channel clock signals in a $f_{op}/2$ case and Fig. 21 shows the first channel sampling clock for the 4 different rates for a $M = 2$ and $N = 32$ scenario.

Fig. 19 Interpolation network architecture

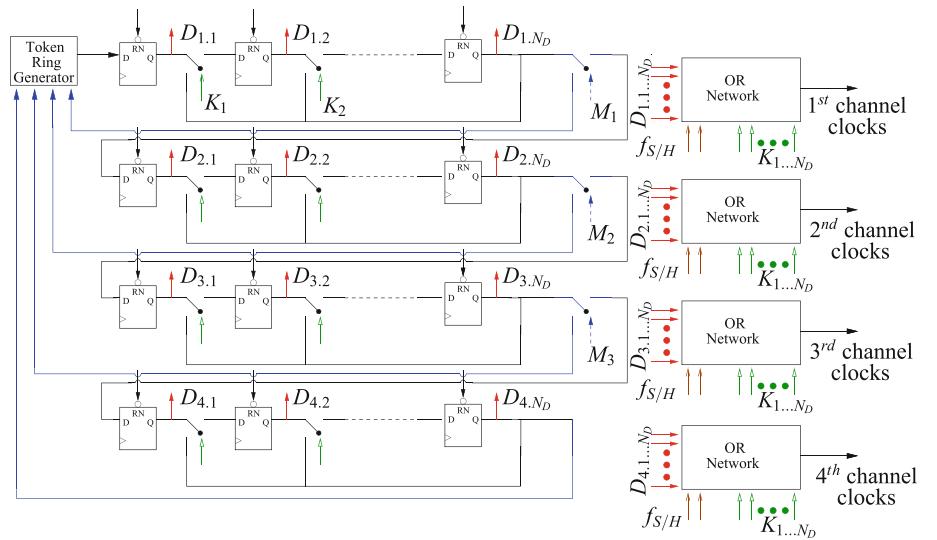
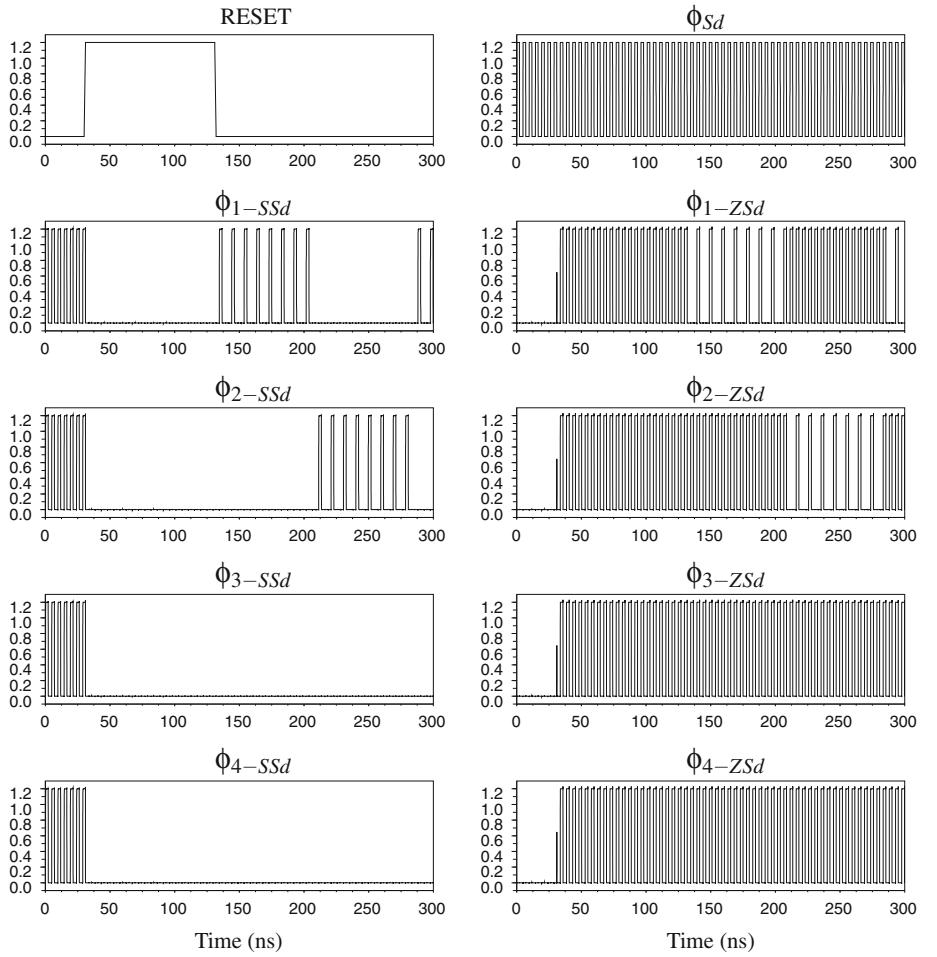


Fig. 20 Clock signals for a $M = 2; K = 16; f_{op}/s$ scenario



6 Prototype

A four channel reconfigurable $TI\Sigma\Delta$ A/D converter employing the proposed interpolation technique has been designed in a 1.2 V 65 CMOS process. The prototype is

suit for GSM, UMTS, EDGE, DVB-T, WiFi and WiMAX standards. The parameters, specifications and results in each scenario are summarized in Tables 1 and 2. The chip total die area including the I/O ring is 3 mm². Its layout is shown in Fig. 22.

Fig. 21 ϕ_{1-ssd} for a $M = 2$; $K = 16$ scenario for the four sampling rates

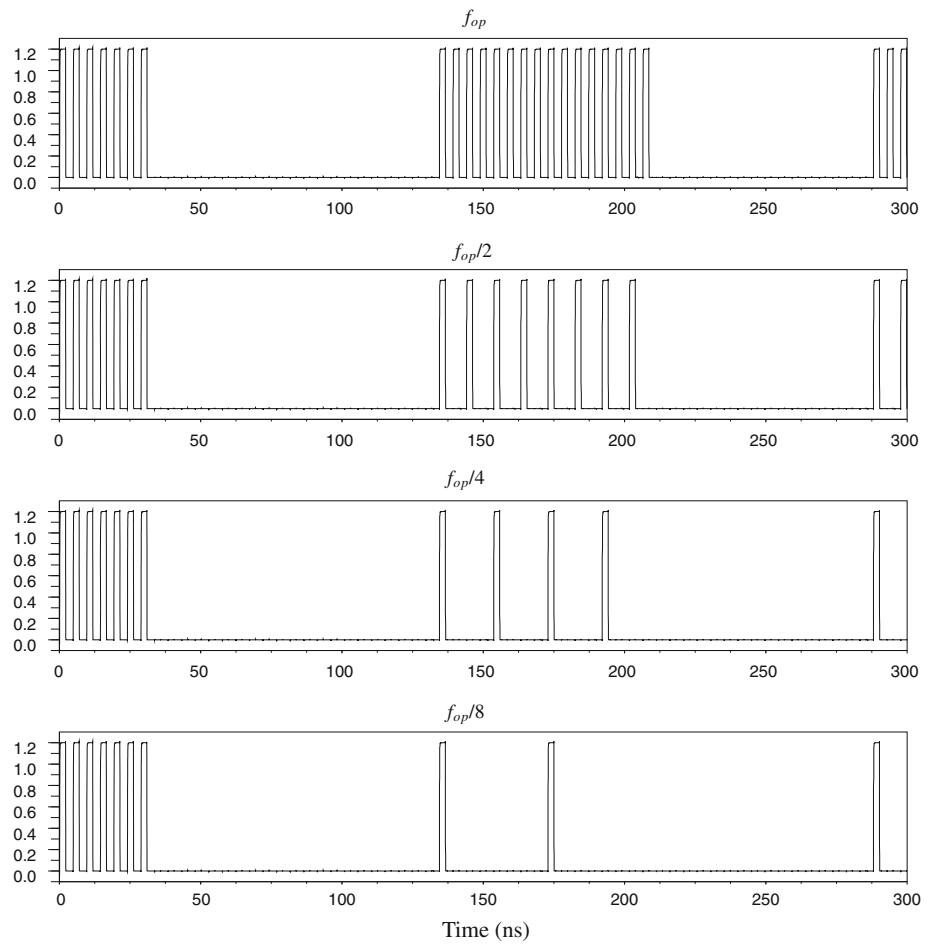


Table 1 Parameters of the implemented four channels $TI\Sigma\Delta$ ADC

Standard	B (MHz)	M	N	Modulator order	f_{op} (MHz)
GSM/EDGE	0.135	1	96	2	26
UMTS/DVBT	4	2	52	4	208
WiFi/WiMax	12.5	4	32	4	208

Table 2 Results of the implemented four channels $TI\Sigma\Delta$ ADC

Standard	SNDR target(dB)	SNDR simulated(dB)	Power(mW) consumption
GSM/EDGE	80	85 ^a	3.108
UMTS/DVBT	80	83 ^b	55.2
WiFi/WiMax	52	53.7 ^a	110.4

^a Results of electrical simulations

^b In the UMTS/DVBT mode, electrical simulations long enough to have a reliable estimation of the SNDR are very time consuming because the interpolation factor and the resolution are high. In fact, in the TI mode, tracing a 2^{13} points spectrum requires a simulation of $2^{13} \times N$ cycles of the complete circuit which requires a very long simulation time. Therefore, for the UMTS/DVBT scenario, the output SNDR was estimated based on the results of electrical simulations of one channel and the results of system level simulations

The analog part of the circuit will not be presented in this paper but it is important to note that when M is lower than four, the inactive channels are turned-off by switching off the biasing current of their OTAs. Thanks to the novel

interpolation technique, $C_{sS/H}$ was downscaled from 54 pF to 8 pF and C_{sI} to 600 fF.

The interpolation network die area is 0.01 mm^2 and its power consumption is 0.32 mW for a $f_{op} = 208 \text{ MHz}$.

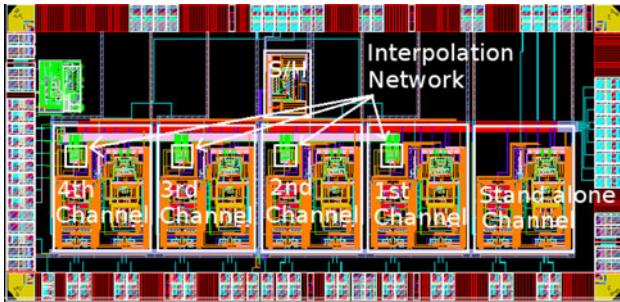


Fig. 22 Circuit layout

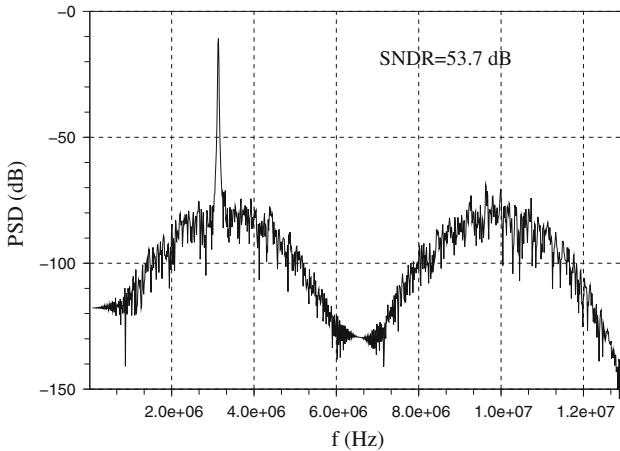


Fig. 23 $T\bar{I}\Sigma\Delta$ output spectrum for the WiFi/WiMax scenario with $NBW = \frac{0.5}{1024}$

This represents only a 15% die increase and a 10% power consumption increase compared to the interpolation network required for the classical technique. Nine external control bits are used to fix M , K and the sampling rate. There are 32 D-flipflops per channel to have N up to 128 when four channels are used.

Figure 23 shows the output spectrum for a WiFi/WiMax scenario obtained with an electrical simulation of the

circuit. The simulation was carried out with the same parameters shown in Table 1. The input signal has an input amplitude of -3.1 dBFS and a frequency of 3 MHz. The measured SNDR is 53.7 dB.

Table 3 shows a qualitative comparison of the $T\bar{I}\Sigma\Delta$ architecture with the new interpolation technique compared to other parallel architectures. The proposed architecture is a good compromise between the considered parameters. However, its performance is limited by channel mismatches resulting from the PVT variations. To overcome this drawback we proposed a novel digital calibration method to compensate gain and offset mismatches. The proposed method takes advantage of the reconstruction digital signal processing on each channel and requires only few logic components for implementation [24, 25].

7 Conclusion

This paper has proposed a new interpolation technique based on the oversampling of the input signal. It allows to reduce capacitor sizes and consequently the required die area compared to the classical interpolation technique. Besides, this new technique decreases the order of the required AAF. Its drawbacks are 15% increase of interpolation network die area and 10% increase of its power consumption compared yet to the classical interpolation technique. In addition, the order of the correction filter is increased from the 10th to the 30th order. Nevertheless, these inconveniences are negligible compared to the acquired benefits.

The proposed interpolation technique was employed in a four channel time interleaved sigma-delta prototype designed in a 1.2 V 65 nm CMOS process. Electrical simulations of the circuit showed that the targeted performance were achieved.

Table 3 Comparison among different parallel $\Sigma\Delta$ A/D converter

Architecture	Die area	Bandwidth to channel mismatch	Sensitivity to process variation	Sensitivity	AAF requirements	Limitation on number of channels	Limitation on modulator architecture	Digital hardware complexity
BF	Very low	Meduim	Meduim	Low	Low	High	High	Very low
FBD	Very high	Very high	Low	Very high	Very low	Low	Low	Very high
$\Pi\Sigma\Delta$	Low	Meduim	High	Low	Very high	Meduim	Low	High
$T\bar{I}\Sigma\Delta$ classical interpolation	High	Meduim	High	Low	Very high	Low	Low	Very low
$T\bar{I}\Sigma\Delta$ new interpolation	Low	High	High	Low	Low	Low	Low	Low

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